Neuromorphic
Computing and
Engineering

PURPOSE-LED
PUBLISHING™

TOPICAL REVIEW • OPEN ACCESS

2D-materials for analog in-memory computing: a device-centric review of advantages and limitations

To cite this article: Jimin Shim *et al* 2026 *Neuromorph. Comput. Eng.* **6** 012003

View the article online for updates and enhancements.

You may also like

- Nonvolatile charge memory with optical controllability in two-terminal pristine - In_2Se_3 nanosheets
Qinliang Li, Cailei Yuan, Ting Yu et al.
- *(Invited)* ALD of Phase Change and Threshold Switching Materials for Next-Generation Nonvolatile Memory Devices
Valerio Adinolfi, Ryan Clarke, Mario Laudato et al.
- Modulating the filament rupture degree of threshold switching device for self-selective and low-current nonvolatile memory application
Xiaolong Zhao, Jiebin Niu, Yang Yang et al.

This content was downloaded from IP address 203.255.190.41 on 22/09/2026 at 01:10

NEUROMORPHIC
Computing and Engineering

Check for updates

OPEN ACCESS

RECEIVED
18 September 2025

REVISED
16 December 2025

ACCEPTED FOR PUBLICATION
17 March 2026

PUBLISHED
27 March 2026

Original content from this work may be used under the terms of the Creative Commons Attribution 4.0 licence.

Any further distribution of this work must maintain attribution to the author(s) and the title of the work, journal citation and DOI.

TOPICAL REVIEW

2D-materials for analog in-memory computing: a device-centric review of advantages and limitations

Jimin Shim[1,4], **Jayoung Yoon**[1,4], **Sookyung Shin**[1,4], **Eunsu Hwang**[1,4], **Dokyoung Lee**[1,2], **Moon-Seok Kim**[3,*] and **Sungho Kim**[1,2,*]

[1] Division of Electronic & Semiconductor Engineering, Ewha Womans University, Seoul 03670, Republic of Korea
[2] Institute for Multiscale Matter and Systems (IMMS), Ewha Womans University, Seoul 03760, Republic of Korea
[3] Department of Semiconductor Convergence, Chungnam National University, Daejeon 34134, Republic of Korea
[4] These authors have equally contributed to this work.
[*] Authors to whom any correspondence should be addressed.

E-mail: kimms@cnu.ac.kr and sunghok@ewha.ac.kr

Keywords: analog switching, 2D-material, 2D-matieral memristors, in-memory computing

Abstract

This review examines the practical advantages of two-dimensional materials for energy-efficient in-memory computing by assembling a curated, experiment-only dataset covering 32 material systems across diverse device structures, mechanisms, and fabrication routes. Energy analysis was standardized using an averaged pulse-based metric, and key figures of merit—switching energy, on/off ratio, endurance, retention, and linearity—were compared against structural and mechanistic factors. Two low-energy-consumption design pathways emerge: ultrathin (<10 nm) two-terminal devices exploiting filament formation for sub-μs updates and three-terminal heterojunction devices leveraging charge trapping to achieve nA-level programming currents over longer timescales. However, dynamic on/off ratios remain modest and are often overstated by DC sweep data. Endurance improves with shorter switching times, and the most intrinsically linear conductance evolution is observed in three-terminal gate-controlled devices employing charge trapping, Schottky barrier modulation, or ion intercalation. No universal optimum exists, as enhancing one performance metric typically compromises another. Based on the comparative analysis presented in this review, three near-term levers emerge as particularly relevant for translating selective material advantages into reproducible system-level gains: standardized pulsed benchmarking, scalable chemical vapor deposition growth with controlled defects and interfaces, and device–circuit co-design.

1. Introduction

The exponential growth of data-intensive applications, particularly artificial intelligence, has increased the demand for high-performance computing [1]. Perception-oriented tasks such as image recognition and natural language processing depend on large-scale matrix operations, with vector–matrix multiplications constituting the computational core of modern neural networks [2]. However, in conventional von Neumann architectures, the physical separation between processing and memory units gives rise to a 'memory wall,' where the latency and energy cost of data movement fundamentally constrain efficiency and scalability [3].

Resistive memory crossbar arrays offer a promising in-memory computing paradigm to overcome the memory wall [4]. In these arrays, the weights are mapped to the conductance states of the nanoscale memory cells located at each crosspoint. Applying input voltages along the word lines yields output currents on the bit lines, thereby executing multiply-and-accumulate operations intrinsically according to Ohm's and Kirchhoff's laws [5]. This co-locating of data and computation significantly reduces off-chip transfers and enables orders-of-magnitude improvements in energy efficiency [6]. Experimental resistive crossbar array systems have demonstrated viability in tasks such as image classification and object

© 2026 The Author(s). Published by IOP Publishing Ltd

detection [7–9]. Nevertheless, system-level scalability, precision, and energy efficiency are ultimately constrained by the analogous resistive switching behavior of memory cells [10, 11]. Achieving stable linear conductance modulation with low variability and long retention is therefore essential to maintain computational accuracy and ensure long-term system endurance [12].

This requirement arises from the fundamental manner in which analog in-memory computing encodes and processes information. In resistive crossbar arrays, synaptic weights are represented not as discrete digital states but as continuous conductance values of individual memory cells. While this analog mapping enables highly parallel vector–matrix multiplication with minimal data movement, it simultaneously renders computation sensitive to device-level non-idealities. Any deviation from proportional and predictable conductance modulation directly manifests as errors in multiply-and-accumulate operations, which accumulate across large arrays and repeated training iterations. At the system level, nonlinear conductance evolution leads to asymmetric weight updates and gradient mismatch during training, whereas device-to-device (D2D) and cycle-to-cycle (C2C) variability introduce stochastic errors that degrade inference accuracy. Limited endurance necessitates frequent write–verify schemes or redundancy at the array level, increasing latency and peripheral circuit overhead, while insufficient retention causes time-dependent drift of stored weights and undermines long-term stability. Together, these effects impose substantial penalties on energy efficiency, throughput, and hardware complexity, offsetting the intrinsic advantages of in-memory computation. Consequently, analog in-memory computing places stringent and interconnected demands on memory devices, requiring low-energy operation, stable retention, high endurance, and, critically, intrinsically linear and reproducible conductance modulation.

Over the past two decades, a broad class of memristive devices (memristors) defined by analog resistive switching has emerged, based on materials such as transition metal oxides, chalcogenide phase-change materials, and ferroelectrics [13]. Among these, metal–oxide memristors constitute an established benchmark that combines analog switching accuracy, reliability, and compatibility with complementary metal–oxide-semiconductor (CMOS) manufacturing [14, 15]. Their operation delivered reproducible conductance modulation, high endurance, and robust retention. High-density oxide crossbar arrays have been fabricated and integrated for direct analog weight updates, achieving exceptional energy efficiency in both training and inference. These results underscore the technological maturity of oxide-based memristors and their central role in the existing in-memory computing hardware [16].

Two-dimensional (2D) materials have also been explored as alternative active layers (figure 1(a)) [17, 18]. Their atomic-scale thickness, dangling-bond-free surfaces, tunable electronic properties, and ability to form van der Waals heterostructures offer the potential for reduced switching voltages, improved D2D uniformity, and access to novel switching mechanisms [19]. Additionally, their mechanical flexibility and chemical stability enable unconventional form factors. Despite these advantages, the reported analog switching performance of 2D-material memristors generally lags behind that of state-of-the-art oxide devices [20], and the CMOS compatibility and high-density integration remain limited. These limitations prompt two key questions: (i) can 2D materials provide a measurable advantage over leading metal–oxide systems for in-memory computing and (ii) can their intrinsic characteristics, specifically their atomic-scale thickness and van der Waals interfaces, be directly leveraged to achieve superior analog switching?

This review provides a focused, evidence-based assessment of these questions. Rather than revisiting the direct comparison of oxide versus 2D-material based memristors discussed elsewhere [20], we concentrate exclusively on the 2D-material domain. Drawing from experimental studies reported over the past decade, we correlate device structures, switching mechanisms, and materials engineering strategies with the stability, linearity, and energy efficiency of analog conductance modulation. Our emphasis is on whether the defining attributes of 2D-materials translate into measurable performance gains under realistic operating conditions. By systematically linking material-level properties to device-level metrics, we comprehensively evaluate the practical potential of 2D-material memristors in next-generation energy-efficient in-memory computing.

In contrast to conventional review articles that primarily compile and qualitatively discuss individual device demonstrations, this work adopts a data-driven, device-centric perspective focused on statistical comparison across a large and heterogeneous experimental literature. By curating experimentally reported analog switching characteristics from leading journals over the past decade and standardizing their evaluation under pulse-driven operation, we aim to identify robust cross-platform trends linking device structure, switching mechanism, and fabrication strategy to practical in-memory computing performance. Consequently, the emphasis of this review is placed on collective distributions and correlations across material systems and device architectures, rather than on detailed schematics or electrical characteristics of individual devices. This methodological stance enables an unbiased assessment of trade-offs

and limitations that are difficult to discern from case-by-case surveys and provides a complementary viewpoint to existing narrative reviews.

Importantly, this statistical perspective is complementary to reviews that emphasize record-breaking or state-of-the-art device demonstrations. While exceptional performance metrics reported in isolated studies are included in our dataset, they are interpreted within the context of their recurrence across independent experiments. Performance characteristics that are not repeatedly observed across multiple studies, material systems, or fabrication routes do not manifest as dominant trends in the statistical distributions and are therefore treated as outliers rather than as representative design rules. This approach prioritizes reproducibility and generality over peak performance, aiming to identify device-level correlations that are more likely to translate into reliable array- and system-level behavior.

2. Scope of analysis

To evaluate analog switching in 2D-material memristors, we compiled a structured survey of the reported device architectures and fabrication methods (table 1). This framework enables direct correlation of key performance indicators with material choices, structural configurations, and processing parameters.

2.1. Structural and fabrication parameters

Devices were categorized according to four attributes:

(1) Active-layer composition: Single-material systems, where the switching medium consists of a single 2D-material, and heterojunction systems, which employ van der Waals heterostructures. This classification captures the influence of interfacial phenomena and band alignment in determining switching.

(2) Device structure: Two-terminal (2T) metal–insulator–metal structures dominated by vertical transport, and three- or multi-terminal (3T) architectures, including memtransistors, which provide gate-tunable conductance and can decouple read and write operations.

(3) Fabrication methods: Mechanical exfoliation, chemical synthesis, and chemical vapor deposition (CVD). This factor is critical for scalability, film uniformity, and defect density.

(4) Geometric parameters: Thickness of the 2D active layer, device area, array size (where applicable). These parameters are essential for contextualizing scaling behavior, integration density, and compatibility with large-scale in-memory computing systems.

2.2. Performance metrics

As discussed in the previous section, matrix multiplication in resistive crossbar arrays requires the mapping of numerical weights directly onto the memristor conductance states. The accuracy and robustness of this mapping largely determine the feasibility of in-memory computing. Five metrics are indispensable for evaluating device performance: energy consumption, on/off ratio, endurance, retention, and linearity (figure 1(b)).

(1) Energy consumption: Energy efficiency is the primary requirement for memristors in crossbar arrays, as switching energy directly governs overall system efficiency. Real-valued weights are typically programmed by iteratively applying voltage pulses until the target conductance is reached. Therefore, minimizing the energy dissipated during the pulse-driven updates is essential. In this review, the switching energy is estimated as the product of the switching voltage, current, and time ($V \times I \times t$) under pulse-train operation, where conductance evolves continuously rather than under quasi-static DC sweeps. In practice, reported parameters are often incomplete or span wide ranges and require careful interpretation. The switching voltage (V_{sw}) and switching time (t_{sw}) are set by the pulse amplitude and duration; however, the SET (potentiation) and RESET (depression) conditions are frequently asymmetric, making energy more accurately expressed as a range rather than a single value. The switching current (I_{sw}) is the most uncertain term, and few studies have directly captured the transient programming current. Instead, the current is often inferred from the conductance at a read bias (V_{read}), introducing uncertainty. Moreover, as the conductance changes continuously during analog switching, the corresponding current varies dynamically. Consequently, the switching energy is summarized here as a bounded interval, $E_{min} = \min(V_{sw}) \times \min(t_{sw}) \times \min(I_{sw})$ to $E_{max} = \max(V_{sw}) \times \max(t_{sw}) \times \max(I_{sw})$. This approach provides a consistent basis

Table 1. Summary of experimentally reported 2D-material memristors, including device structure, fabrication method, thickness, switching mechanism, and key performance metrics (energy, on/off ratio, endurance, retention, linearity).

2D material	Device structure	Fabrication method	Thickness (nm)	Device area (μm^2) (array size)	Mechanism	Energy consumption (J) (min/max)	On/Off ratio	Endurance (cycles)	retention (s)	Linearity	Year [references]
MoS_2	2T	Exfoliation	15	10	Vo migration (S)	$8 \times 10^{-9}/5.3 \times 10^{-8}$	1.75	6000	10^5		2018 [21]
MoS_2	3T	CVD	0.65	500	Vo migration (S)	$6 \times 10^{-10}/1.4 \times 10^{-8}$	22.5	500	8.64×10^4		2018 [22]
MoS_2	3T	Exfoliation	6.5	NA	Ion intercalation (Li)	$9 \times 10^{-12}/3.3 \times 10^{-10}$	36.6	600	3000	△	2019 [23]
MoS_2	3T	CVD	0.65	12	Vo migration (S)	$7.5 \times 10^{-9}/3 \times 10^{-8}$	4	840	NA		2019 [24]
MoS_2	2T	CVD	1.3	4	Filament formation (Cu ion)	$8.6 \times 10^{-9}/1.1 \times 10^{-8}$	1.27	80	NA		2019 [25]
MoS_2	2T	Exfoliation	40	NA	Phase transition (Li ion)	$1.2 \times 10^{-10}/6 \times 10^{-10}$	5	1000	8000	△	2019 [26]
MoS_2	3T	CVD	0.65	0.63 (10 × 9)	Charge trapping & SBM (S Vo)	$3 \times 10^{-11}/9.8 \times 10^{-10}$	32.5	250	8.64×10^4	△	2020 [27]
MoS_2	2T	CVD	35	NA	Filament formation (Ag ion)	NA	6	400	NA		2020 [28]
MoS_2	3T	Exfoliation	15	10	SBM (S Vo)	$9 \times 10^{-10}/3.3 \times 10^{-8}$	11	6000	NA	△	2020 [29]
MoS_2	3T	CVD	0.65	8 (10 × 10)	Vo migration (S)	$2.4 \times 10^{-13}/1.7 \times 10^{-12}$	7	1000	4.8×10^4		2021 [30]
MoS_2	2T	Exfoliation	7	16	Vo migration (S or O)	$1.8 \times 10^{-7}/2.7 \times 10^{-5}$	3	1000	10^4	O	2021 [31]
MoS_2	3T	CVD	0.7	500	Charge trapping (S Vo)	NA	1.3	60	NA		2021 [32]
MoS_2	3T	CVD	2.1	NA	Phase transition ion intercalation (Li)	$6 \times 10^{-9}/2.6 \times 10^{-8}$	4.4	10^6	NA	△	2022 [33]
MoS_2	2T	Exfoliation	2.6	25 (6 × 6)	Filament formation (S Vo)	$3 \times 10^{-14}/3.7 \times 10^{-11}$	110	10^7	NA	O	2022 [34]
MoS_2	2T	CVD	2	25 000	SBM (O Vo)	$1.6 \times 10^{-9}/1.3 \times 10^{-8}$	8	2000	7000		2022 [35]
MoS_2	2T	CVD	2.1	100 (4 × 4)	Filament formation (Ag ion)	$9 \times 10^{-6}/2.4 \times 10^{-5}$	2.67	500	10^4		2022 [36]
MoS_2	2T	Sputtering	5	900	SBM (S Vo)	$2.5 \times 10^{-10}/5.4 \times 10^{-9}$	2.18	400	10^4		2023 [37]
MoS_2	2T	Exfoliation	NA	NA	SBM (O ion)	$1.6 \times 10^{-11}/1.6 \times 10^{-10}$	8	800	NA		2023 [38]
MoS_2	3T	CVD	0.65	50 (2 × 2)	Charge trapping (floating gate)	$2.8 \times 10^{-9}/2.2 \times 10^{-6}$	6.85	5000	1000	O	2023 [39]
MoS_2	2T	Sulfurization	1.4	1	Filament formation (Au)	$9.2 \times 10^{-10}/3.1 \times 10^{-9}$	1.13	400	10^4	O	2024 [40]
MoS_2	2T	Exfoliation	15	10	Vo migration (S)	$7.5 \times 10^{-9}/1.6 \times 10^{-8}$	2.16	4000	NA		2025 [41]
hBN	2T	CVD	8	9 (1 × 10)	Filament formation (Ti ion)	$1 \times 10^{-13}/4.5 \times 10^{-13}$	3.3	10^4	10^4		2022 [42]
hBN	2T	CVD	2	40 000	Filament formation (B Vo)	$3.4 \times 10^{-8}/7.1 \times 10^{-8}$	1.36	1000	1000	△	2022 [43]
hBN	2T	CVD	5	9 (1 × 10)	Filament formation (Ti ion)	$2.7 \times 10^{-13}/7.7 \times 10^{-13}$	2.33	6000	10^4		2023 [44]
hBN	2T	CVD	10	9 (1 × 10)	Filament formation (Ti ion)	$1.8 \times 10^{-12}/7 \times 10^{-12}$	3.33	3000	10^4		2023 [45]

(Continued.)

Table 1. (Continued.)

hBN	2T	Sputtering	NA	NA	Filament formation (Cu ion)	$1.9 \times 10^{-6}/7.2 \times 10^{-6}$	4	160	NA		2024 [46]
hBN	2T	CVD	2.7	15 000	Filament formation (Ag ion)	$1.5 \times 10^{-16}/6 \times 10^{-15}$	30	10^4	1000		2024 [47]
hBN	2T	CVD	7.44	400 (16 × 16)	Filament formation (Cu ion)	$8.3 \times 10^{-10}/2.8 \times 10^{-6}$	2.5	10^5	10^4	O	2025 [48]
hBN	2T	CVD	3.34	25	Filament formation (Ti ion)	$3.5 \times 10^{-11}/2.3 \times 10^{-10}$	4.4	128	1000	O	2025 [49]
WSe_2	3T	Exfoliation	33.6	22 000	Ion intercalation (Li)	$5 \times 10^{-12}/3.3 \times 10^{-11}$	2.2	350	5000	△	2018 [50]
WSe_2	2T	CVD	3.4	NA	Filament formation (W Vo)	$2 \times 10^{-10}/3.6 \times 10^{-9}$	18	2000	4×10^4		2021 [51]
WSe_2	3T	Exfoliation	16	120	Adsorption of H_2O, O_2 & charge trapping (WSe_2/SiO_2 interface)	$2.5 \times 10^{-6}/8 \times 10^{-6}$	3.2	3600	500	△	2021 [52]
WSe_2	3T	Exfoliation	6	NA	SBM (Se Vo)	$2.7 \times 10^{-9}/9.9 \times 10^{-9}$	3.66	100	300		2022 [53]
WSe_2	3T	Exfoliation	10	1.92	SBM (Se Vo)	$1.5 \times 10^{-9}/4 \times 10^{-9}$	2.66	10^4	10^4	△	2023 [54]
WS_2	2T	Spin coating	65	NA	Filament formation (Ag ion)	$3.5 \times 10^{-15}/7.2 \times 10^{-13}$	100	10^9	4×10^4		2019 [55]
WS_2	2T	Sputtering	120	(3 × 3)	Charge trapping (O Vo)	$1 \times 10^{-9}/1.3 \times 10^{-7}$	100	1.5×10^4	NA		2019 [56]
K-MnO_2	2T	CVD	26	200	Phase transition (K ion)	$5.6 \times 10^{-12}/6.8 \times 10^{-11}$	12	5600	NA		2021 [57]
$ZnPS_3$	2T	Exfoliation	4	4	Filament formation (Ag ion)	$1 \times 10^{-18}/4 \times 10^{-11}$	2×10^7	10^4	3.6×10^4	O	2025 [58]
$CuInP_2S_6$	2T	Exfoliation	167	100 (3 × 3)	Ferroelectric polarization & charge trapping (Cu Vo)	$3 \times 10^{-11}/4.5 \times 10^{-9}$	30	140	2000		2020 [59]
GaSe	2T	Exfoliation	17	NA	Filament formation (Cu ion)	$1.4 \times 10^{-11}/4.4 \times 10^{-6}$	3.14×10^5	200	NA		2025 [60]
Gr	3T	Exfoliation	8	60	Ion intercalation (Li)	$5 \times 10^{-13}/4 \times 10^{-12}$	8	6000	5×10^4	△	2018 [61]
Gr	3T	Exfoliation	0.34	50	Ferroelectric polarization	$2 \times 10^{-3}/6 \times 10^{-3}$	1.75	400	NA		2019 [62]
Gr	3T	Exfoliation	0.34	NA	Hydrogenation of Gr with H^+ ions	$8 \times 10^{-12}/7 \times 10^{-7}$	3.5×10^5	80	NA		2024 [63]
Gr	3T	CVD	0.34	200	Charge trapping (floating gate)	$2.5 \times 10^{-10}/1.2 \times 10^{-9}$	2.4	10^4	10^5	△	2025 [64]
$MoSe_2$	3T	Exfoliation	2.9	50 (2 × 8)	SBM (K, Au ions)	$7.5 \times 10^{-13}/4.5 \times 10^{-12}$	6	800	3.6×10^4	△	2025 [65]
$MoTe_2$	3T	Exfoliation	7	16 (4 × 4)	Charge trapping (SiN_x)	$1.5 \times 10^{-6}/3 \times 10^{-5}$	20	1.2×10^4	NA	△	2021 [66]
$PdSe_2$	2T	Exfoliation	3	4 (5 × 5)	Filament formation (Ti ion)	$3.2 \times 10^{-9}/5.8 \times 10^{-9}$	1.6	200	8.64×10^4		2021 [67]
ReS_2	2T	Exfoliation	3	NA	SBM (S Vo)	$7.5 \times 10^{-9}/2.7 \times 10^{-8}$	3.6	80	700		2021 [68]
ReS_2	2T	Exfoliation	9	NA	Filament formation (O ion)	$8.9 \times 10^{-14}/3.4 \times 10^{-12}$	10	200	1000	O	2022 [69]
SnS	2T	CVD	3.7	NA	Ferroelectric polarization	$1.5 \times 10^{-11}/1.1 \times 10^{-9}$	20.5	10^4	1000	O	2020 [70]
SnS	2T	Exfoliation	13	2500 (32 × 32)	Filament formation (Ag ion)	$2.1 \times 10^{-13}/4.5 \times 10^{-12}$	10	10^4	10^5	O	2021 [71]
SnS_2-RGO	T	Chemical reaction	600	NA	Ion intercalation (Na)	$1.3 \times 10^{-10}/7.3 \times 10^{-9}$	1.16	3500	NA	O	2019 [72]
SnS_2	3T	Exfoliation	20	16	Charge trapping (bulk trap)	$1.3 \times 10^{-9}/1.4 \times 10^{-8}$	11	10^5	10^6		2022 [73]

(Continued.)

Table 1. (Continued.)

2D material	Device structure	Fabrication method	Thickness (nm)	Device area (μm^2) (array size)	Mechanism	Energy consumption (J) (min/max)	On/Off ratio	Endurance (cycles)	retention (s)	Linearity	Year [references]
$Ti_3C_2T_x$	2T	Exfoliation	150	NA	Charge trapping (Ti and O vacancies)	$4 \times 10^{-11}/5.4 \times 10^{-10}$	4.5	10^6	10^5		2019 [74]
α-MoO_3	3T	Exfoliation	12.6	NA	Electrochemical proton doping	$6.3 \times 10^{-12}/1.2 \times 10^{-11}$	1.35	500	50	△	2017 [75]
α-MoO_3	3T	Exfoliation	18	25	Ion intercalation (Li)	$2.5 \times 10^{-9}/4.4 \times 10^{-9}$	1.75	4000	100	△	2018 [76]
SnO_2	3T	Liquid metal printing	2	15 000	SBM (O Vo)	$4.5 \times 10^{-10}/6.8 \times 10^{-10}$	1.5	1000	10^4		2021 [77]
PO_x/BP/PO_x	3T, hetero	Exfoliation	2/14/2	NA	Charge trapping (PO_x/BP interface)	$1.8 \times 10^{-7}/4.6 \times 10^{-7}$	1.25	40	NA		2016 [78]
BP/SnSe	3T, hetero	Exfoliation	6/100	NA	Charge trapping (PO_x/BP interface)	$6 \times 10^{-8}/2 \times 10^{-7}$	1.4	40	NA		2017 [79]
hBN/MoS_2/hBN/MoS_2	3T, hetero	Exfoliation	13.7/7.1/8.2/12.4	NA	Charge trapping (floating gate)	NA	1.5	NA	10^4		2018 [80]
WSe_2/Gr	3T, hetero	Exfoliation	20-50/NA	25	Redox reaction & SBM (WSe_2/Gr interface)	$2.5 \times 10^{-13}/2.8 \times 10^{-8}$	1750	1000	1000		2018 [81]
WSe_2/hBN	3T, hetero	Exfoliation	2/20	25	Charge trapping (WCL)	$9 \times 10^{-13}/1.6 \times 10^{-11}$	5.16	1200	NA		2018 [82]
hBN/MoS_2/hBN/Gr	3T, hetero	CVD & exfoliation	15/0.65/15/NA	27	Charge trapping (floating gate)	$1.2 \times 10^{-13}/1.2 \times 10^{-11}$	100	300	1000	O	2020 [83]
WSe_2/$MoTe_2$	3T, hetero	Exfoliation	5-6/5-6	NA	Charge trapping (WSe_2/$MoTe_2$ interface)	$2.4 \times 10^{-13}/3 \times 10^{-11}$	200	200	10^4		2020 [84]
MoS_2/Nb_2O_5	3T, hetero	CVD & sputtering	2/2.1	25 000	SBM	$7.5 \times 10^{-11}/9 \times 10^{-11}$	1.2	2000	1000	△	2021 [85]
hBN/In_2Se_3	3T, hetero	Exfoliation	20/40	175	Ferroelectric polarization	$1.5 \times 10^{-14}/1.5 \times 10^{-13}$	10	500	500		2021 [86]
$PdSeO_x$/$PdSe_2$	2T, hetero	Exfoliation & UV treatment	2.2	4	Filament formation (Ti ion)	$3.2 \times 10^{-11}/1 \times 10^{-8}$	150	700	8.64×10^4	O	2022 [87]
MoO_x/MoS_2/hBN	3T, hetero	Exfoliation & UV treatment	3/10-20/NA	NA	Charge trapping (MoO_x/MoS_2 interface)	$3.6 \times 10^{-17}/2.16 \times 10^{-16}$	2	1440	NA		2023 [88]
MoS_2/hBN/Gr	3T, hetero	CVD & exfoliation	0.65/7/0.34	100(9 × 3)	Charge trapping (floating gate)	$6.2 \times 10^{-12}/3.6 \times 10^{-10}$	60	10^4	1000	△	2023 [89]
MoS_2/WSe_2	3T, hetero	Exfoliation	10/6.5	NA	SBM (charge trapping)	$1.1 \times 10^{-10}/1.1 \times 10^{-9}$	10	400	NA		2024 [90]

Gr: Graphene, NA: not available, hetero: heterojunction, Vo: vacancy, SBM: Schottky barrier modulation.

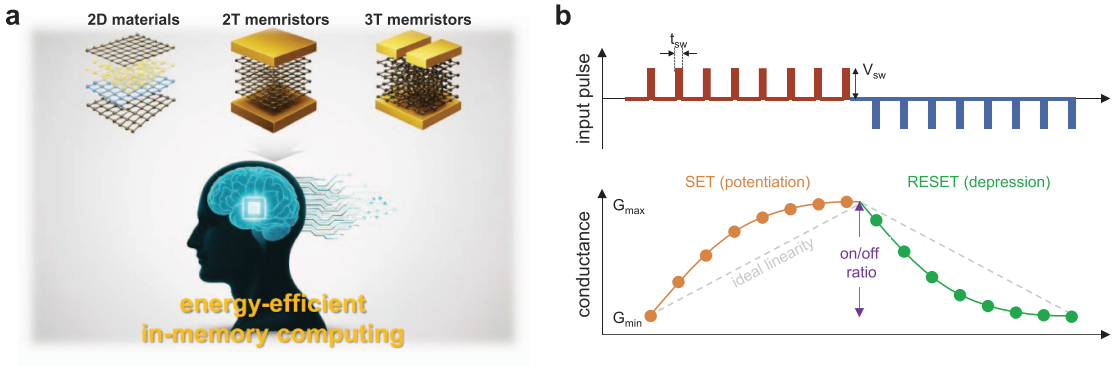


Figure 1. Conceptual overview of 2D-material memristors for energy-efficient in-memory computing. (a) Illustration of 2D materials, memristive devices, and crossbar array architectures integrated for neuromorphic hardware. (b) Schematic of pulse-driven analog switching, where repeated SET (potentiation) and RESET (depression) pulses modulate conductance between G_{min} and G_{max}. Key performance indicators include switching time (t_{sw}), switching voltage (V_{sw}), on/off ratio, and linearity of conductance evolution.

for cross-study comparisons while explicitly accounting for variability in pulse-driven analog switching of 2D-material memristors.

(2) On/off ratio: The on/off ratio defines the effective dynamic conductance range available for weight encoding in crossbar arrays. Values extracted from DC I–V measurements can substantially overestimate the performance of analog operations. Here, the on/off ratio is defined as the conductance ratio G_{max}/G_{min} (equivalently, I_{on}/I_{off} at V_{read}), where G_{max} and G_{min} are the highest and lowest stable states, respectively, achieved under the pulse protocols used for analog mapping. A larger on/off ratio improves the read signal-to-noise ratio, reduces quantization errors in sense circuits, and mitigates misclassification due to D2D and C2C variability. However, excessively high ratios often accompany abrupt transitions that degrade linearity and update symmetry, thereby reducing training accuracy. Thus, the on/off must be balanced with linearity, energy, and endurance, rather than treated as an isolated figure of merit.

(3) Endurance: This quantifies the number of pulse-driven conductance-modulation cycles a device can sustain without degradation of analog characteristics. Because accurate weight mapping requires highly reproducible updates under repeated pulse streams, memristors for in-memory computing require stricter endurance than conventional memories. Systematic endurance testing remains uncommon in the 2D-material memristor, and the reported conditions often differ from those used for analog switching demonstrations, complicating comparisons. We therefore apply the following protocol: for studies without a dedicated endurance analysis, we record the maximum number of analog switching repetitions explicitly demonstrated (typically $\leqslant 10^3$ cycles). For studies reporting separate endurance tests, the highest cycle count was extracted as an upper-bound indicator of durability, annotating cases in which the test conditions diverged from the analog switching protocol.

(4) Retention: This quantifies the stability of the programmed conductance states over time under the specified temperature and read-bias conditions. In conventional memory technologies, accelerated tests are performed at elevated temperatures (85 °C or 125 °C), with targets of $\geqslant 10^5$–10^6 s of stable state retention. By contrast, many 2D-material memristor studies omit retention measurements, and those that often report only room-temperature results in approximately 10^2–10^4 s range. Consequently, relative to other material platforms, retention, and thus the long-term reliability of analog switching, remains insufficiently characterized for 2D systems. Therefore, in this review, we focus on studies demonstrating comparatively stable retention and analyze the material, structural, and processing factors that appear to enhance the state stability under the reported conditions.

(5) Linearity and variable pulse schemes: Linearity describes the proportional evolution of conductance with the number of identical pulses. An ideal linear memristor exhibits uniform increases during potentiation and decreases during depression. High linearity ensures predictable weight-to-conductance mapping, reduces circuit and write–verify overheads, and improves training efficiency, whereas strong nonlinearity necessitates calibration or adaptive models, increases complexity, and hinders convergence. In contrast to metal–oxide memristors, for which linearity has been

systematically engineered, quantitative studies on 2D-material memristors remain scarce. The reported improvements often rely on amplitude-variable pulse schemes, including ramped envelopes, pulse widths, or duty-cycle modulation under current compliance, gate-assisted modulation, and closed-loop write–verify control. Given the inconsistent definitions and protocols across studies, rigorous numerical comparisons are not yet possible. Therefore, this review focuses on qualitative insights and identifies recurring strategies that consistently correlate with improved linearity in 2D-material memristors.

2.3. Excluded topics

An emerging class of memristors uses the intrinsic direct bandgap of 2D-materials to exploit their optical properties [91, 92]. In these devices, optical stimuli, applied either independently or in conjunction with electrical pulses, are used to efficiently modulate conductance. Although this approach offers additional operational degrees of freedom, it was excluded from this review for three reasons.

First, no standardized protocol exists for the applied optical inputs across reported studies, including parameters such as wavelength, intensity, and exposure duration. This lack of uniformity precludes a direct and quantitative comparison of the analog switching performances. Second, the number of published studies was limited, preventing statistically meaningful conclusions. Third, the mechanisms underlying the optically induced switching are not well established. Most reports attribute the observed conductance modulation to photogenerated carriers but provide only qualitative explanations without mechanistic rigor. Clarifying these processes requires systematic investigation. Therefore, the scope of this review is restricted to electrically driven switching phenomena in 2D-material memristors.

3. Data set overview

Table 1 presents a curated dataset of 2D-material memristors reported over the past decade, covering 32 distinct material systems. The dataset was drawn exclusively from experimental studies and recorded the device structure, fabrication method, active-layer thickness, switching mechanism, and key analog performance metrics. As illustrated in figure 2(a), two-terminal (2T) vertical structures accounted for 33 cases, whereas three-terminal (3T) memtransistor-type architectures accounted for 24. An additional 13 devices incorporated van der Waals heterojunctions in both the 2T and 3T configurations. Nearly 70% of the reported devices employ conventional 2T/3T designs, whereas the rest exploit heterostructured interfaces.

Fabrication approaches (figure 2(b)) were dominated by mechanical exfoliation (35 cases) and CVD (22 cases). Less common methods include sputtering, sulfurization, spin coating, liquid metal printing, and chemical conversion. This distribution underscores the predominantly laboratory-scale character of the current research and highlights the challenge of advancing toward large-area CMOS-compatible syntheses.

Switching mechanisms can be categorized into six principal types (figure 2(c)): filament formation, charge trapping, Schottky barrier modulation (SBM), vacancy migration, ion intercalation, and others (including ferroelectric polarization or phase transition). Distinct correlations with the device structure are evident (figure 2(d)). For 2T devices, filamentary conduction dominates, with 21 reported cases indicating that the conductance modulation is most often governed by the formation and rupture of ion- or vacancy-mediated filaments bridging the two electrodes. By contrast, no filamentary mechanism has been reported for 3T devices, which rely on diverse processes, such as charge trapping, SBM, and ion intercalation. Charge trapping is the prevailing mechanism in heterojunction-based devices, reflecting the frequent exploitation of interface traps formed at the junctions between dissimilar 2D-materials.

Although most studies report at least one performance metric, such as the switching energy, on/off ratio, endurance, retention, or linearity, a comprehensive characterization across all metrics remains rare. Endurance and retention data are particularly limited, and linearity is generally discussed qualitatively in the context of pulse-scheme optimization, rather than through standardized numerical benchmarks. Consequently, the dataset offers a diverse yet uneven basis for assessing how intrinsic material properties and device architectures govern the analog switching behavior. In the following sections, we leverage this dataset to compare the performance metrics and evaluate whether the atomic-scale thickness and van der Waals interfaces of 2D-materials provide tangible advantages over conventional material platforms.

Importantly, this unevenness is not merely a limitation of data availability but reflects the intrinsic heterogeneity of the reported devices. Even within nominally identical material systems, switching mechanisms, electrode configurations, and performance metrics vary widely across studies, preventing

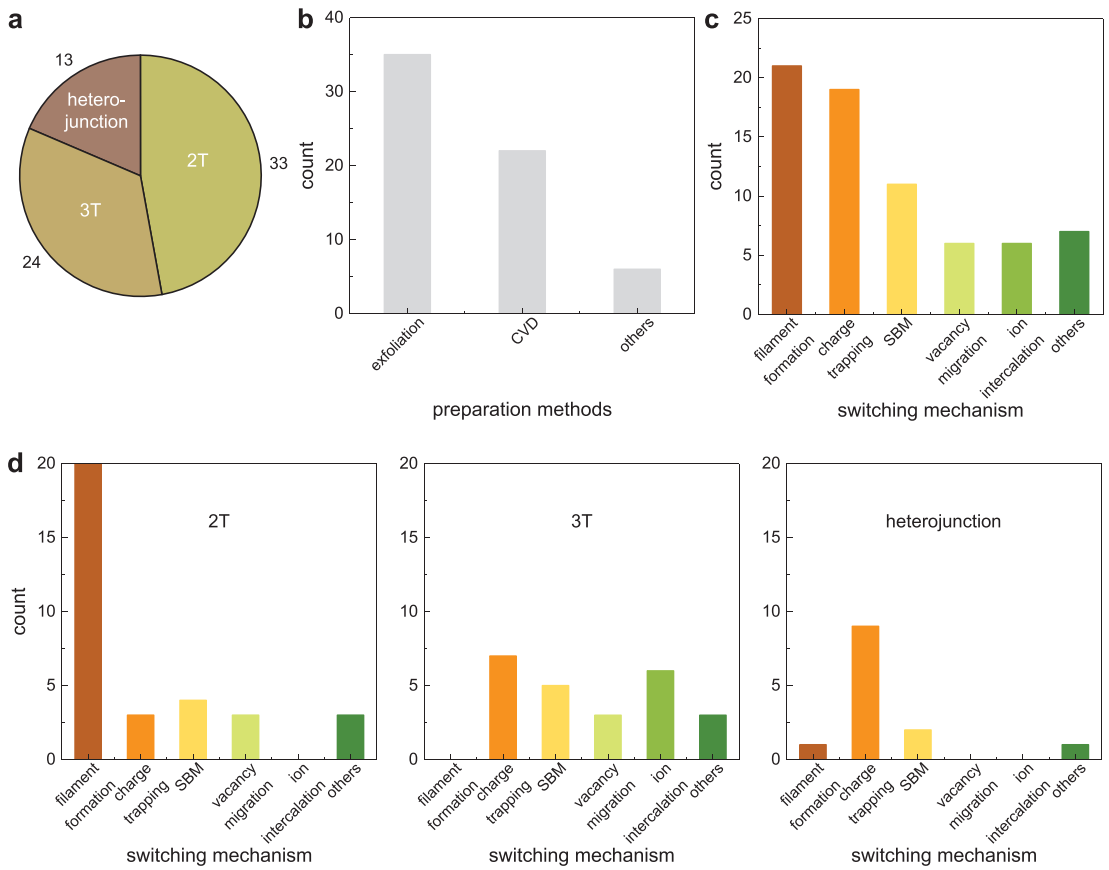


Figure 2. Overview of the curated dataset of 2D-material memristors. (a) Distribution of device structures (2T, 3T, and heterojunction). (b) Reported preparation methods, dominated by exfoliation and CVD. (c) Classification of switching mechanisms, including filament formation, charge trapping, Schottky barrier modulation (SBM), vacancy migration, ion intercalation, and others. (d) Correlation between switching mechanism and device structure, showing filament formation prevalent in 2T devices, whereas 3T and heterojunction architectures predominantly rely on charge trapping, SBM, or ion intercalation.

straightforward material- or process-centric generalization. As a result, statistically meaningful correlations emerge only in limited cases where trends are repeatedly observed across independent reports. In contrast, parameters for which no such recurring behavior is identified are not further generalized or causally interpreted in this review.

As a result of this diversity, the compiled performance metrics span wide dynamic ranges and naturally include extreme values. In the present analysis, such extreme cases are not excluded but are statistically identified as outliers when they do not reflect recurring behavior across the broader literature. The absence of repeated reproduction across independent reports implies that these cases do not define the central tendency of device performance. Accordingly, the subsequent analyses focus on median values and interquartile trends, which more reliably capture reproducible and scalable characteristics relevant to practical analog in-memory computing. In the following sections, we leverage this dataset to compare performance metrics only where statistically supported trends exist and to explicitly delineate the current limits of generalization in 2D-material memristor research.

4. Comparative analysis of performance metrics

4.1. Switching energy

The energy consumed per potentiation or depression event (hereafter referred to as the switching energy) is the most direct indicator of the efficiency of 2D-material memristors for in-memory computing because such events accumulate over billions of weight updates. As summarized in table 1, the conductance during analog switching does not remain constant but evolves within a defined range. Accordingly, the switching energy spanned an interval rather than a single value. To enable a consistent comparison, we defined the average switching energy (E_{avg}) as the arithmetic mean of the reported

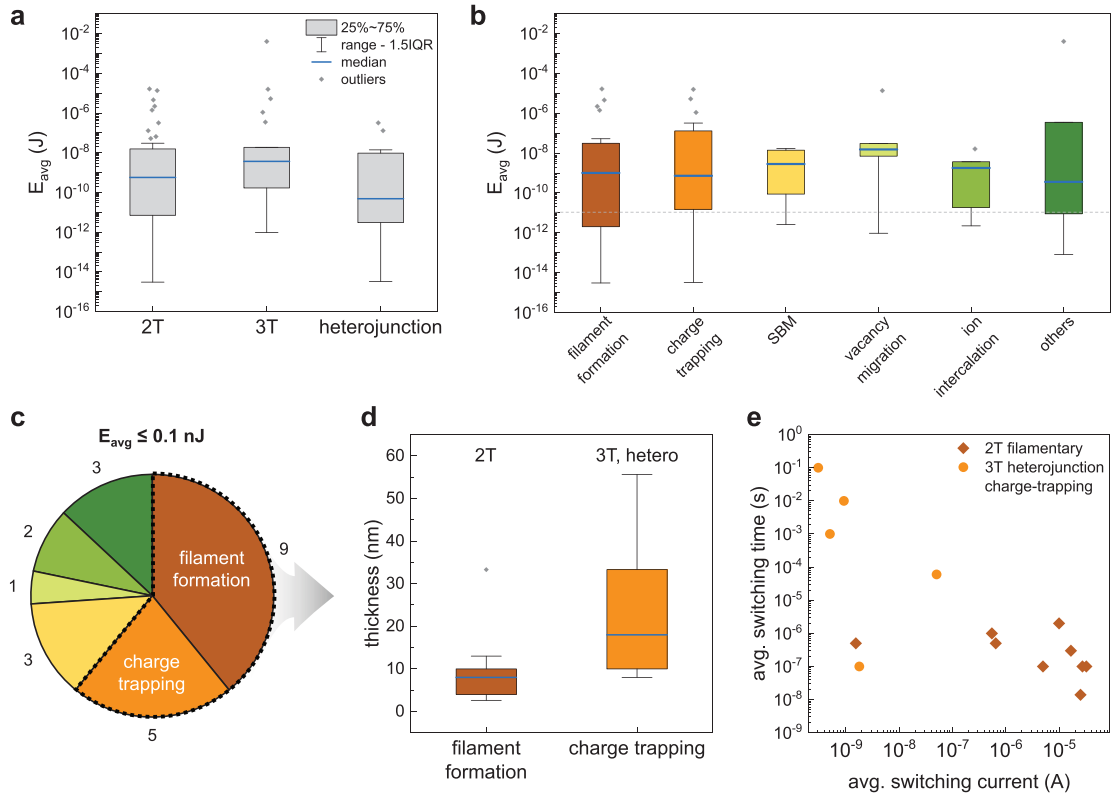


Figure 3. Comparative analysis of switching energy in 2D-material memristors. (a) Box plots of average switching energy (E_{avg}) categorized by device structure (2T, 3T, heterojunction). Each box spans the interquartile range (25%–75%), the horizontal line indicates the median, whiskers represent 1.5 × IQR (interquartile range), and dots denote outliers. (b) Distribution of E_{avg} across switching mechanisms, highlighting filament formation and charge trapping as lower-energy pathways. (c) Mechanistic breakdown of devices with $E_{avg} \leqslant 0.1$ nJ, dominated by filament formation (2T) and charge trapping (3T heterojunctions). (d) Active-layer thickness distributions for low-energy devices, showing ultrathin layers in 2T filamentary cases and thicker layers in 3T charge-trapping devices. (e) Trade-off between average switching current and switching time, where 2T filamentary devices achieve rapid sub-μs updates at higher currents, whereas 3T heterojunction charge-trapping devices operate at nA currents with longer switching times.

minimum and maximum values for each device; all subsequent analyses in this review were based on this averaged metric.

Figure 3(a) separates the dataset by device structure, presenting box plots of E_{avg} for the 2T, 3T, and heterojunction devices. All three categories exhibited broad distributions, reflecting the intrinsic diversity of switching mechanisms and reporting conditions. Excluding outliers, no clear structural advantage emerged as the interquartile ranges of the 2T, 3T, and heterojunction devices largely overlapped. A modest difference is observed for the heterojunction devices, which show a slightly lower median E_{avg} (blue line) than their 2T and 3T counterparts. This suggests that although structural design alone does not guarantee a significant energy reduction, heterostructure interfaces may confer incremental benefits under specific switching conditions.

Figure 3(b) reorganizes the dataset using a switching mechanism. Although the overall energy distributions show substantial overlap across different switching mechanisms, median values indicate that filament formation and charge trapping are more frequently associated with lower switching energies. This tendency becomes more evident when focusing on the lowest-energy subset ($E_{avg} \leqslant 0.1$ nJ), as shown in figure 3(c). Within this subset, most cases corresponded to filament formation (nine cases) or charge trapping (five cases). Notably, filament formation occurred exclusively in 2T structures, whereas charge trapping was consistently achieved in 3T heterojunction configurations. These findings highlight specific structure–mechanism pairings as dominant pathways for minimizing the switching energy within the current experimental dataset.

Material thickness further differentiated these low-E_{avg} cases. For 2T filamentary devices, the active 2D layers were almost uniformly thinner than 10 nm (figure 3(d)), underscoring the critical role of ultrathin channels in confining ionic/vacancy transport and reducing the switching energy. By contrast, 3T heterojunction charge-trapping devices typically employ much thicker active layers, suggesting that

extended thicknesses stabilize the interfacial trap distributions or favor floating gate formation, thereby enabling gate-tunable analog switching with modest energy costs. A comparison of the switching current and switching time for the two dominant low-E_{avg} categories further illustrates their trade-offs (figure 3(e)). Most 2T filamentary devices switch extremely rapidly, typically within 1 μs, but require relatively high currents on the order of approximately 1 μA. By contrast, 3T heterojunction charge-trapping devices operate with very low switching currents (approximately 1 nA) yet demand substantially longer switching times.

Taken together, these observations suggest two viable strategies for achieving low switching energy in 2D-material memristors. The first is the use of ultrathin (<10 nm) layers in 2T structures, exploiting filament formation to minimize energy through short switching times despite the higher current demands. The second is the implementation of 3T heterojunction configurations, in which interfacial traps or floating gates enable charge trapping as the dominant mechanism. Although this approach requires longer switching times, a markedly reduced programming current yields comparably low energy consumption. Moreover, the gate control intrinsic to 3T devices provides an additional degree of freedom, enabling enhanced conductance modulation via optimized combinations of gate and drain biases.

4.2. On/off ratio

As summarized in table 1, most 2D-material memristors exhibit on/off ratios below 10, which are markedly lower than those reported for other material platforms. This limited dynamic range fundamentally constrains their suitability for reliable weight encoding in crossbar arrays, where a clear separation of the conductance states is essential for accurate analog computation. A few studies [59, 61, 64] demonstrated unusually large on/off ratios; however, these values were predominantly achieved by suppressing the minimum conductance state to extremely low levels. Although this practice artificially inflates the on/off ratio, it simultaneously reduces the read current under the applied read bias to magnitudes approaching or even below the detection limit of the sense amplifiers. In such regimes, the current becomes indistinguishable from noise or necessitates complex peripheral amplification circuitry, both of which undermine the intended energy and area efficiencies of in-memory computing architectures. Consequently, the large on/off ratios obtained through the abnormal suppression of the minimum conductance cannot be regarded as a significant performance advantage for 2D-material memristors from a system-level in-memory computing perspective.

Another limitation of the existing research is the frequent failure to distinguish between the on/off ratios extracted from quasi-static DC sweeps and those measured under pulsed operation. Reports highlighting high on/off ratios often rely solely on DC sweep data, which are not representative of actual device operations during in-memory computing tasks. By contrast, when the same devices are subjected to pulse-train inputs to probe dynamic conductance modulation, the on/off ratios are typically much smaller. This discrepancy underscores a critical gap: the parameter of real technological relevance is not the static ratio derived from DC sweeps but rather the dynamic range sustained under repeated pulsed operation, which dictates the precision and linearity of weight updates in practical arrays. However, a rigorous and standardized evaluation of the pulsed on/off ratio in 2D-material memristors remains largely absent, leaving their true suitability for large-scale in-memory computing unresolved.

To further investigate whether certain materials or architectures offer advantages, we analyzed all the reported cases with on/off ratios exceeding 20. Only 14 devices satisfied this criterion, representing a small fraction of the total dataset. Within this subset, no systematic dependence on the device architecture was observed, indicating that structural variations such as 2T, 3T, or heterojunctions do not inherently promote higher ratios (figure 4(a)). Instead, most of these devices rely on resistive switching mechanisms associated with filament formation or charge trapping (figure 4(b)), indicating that these mechanisms are capable of producing an abrupt conductance contrast. In terms of materials, MoS2 and WS2 appeared more frequently among the reported high-ratio cases (figure 4(c)), reflecting both their prevalence in the literature and the relative maturity of their synthesis and device integration processes. However, the sample size of 14 devices was insufficient to establish a statistically meaningful trend, and the apparent material preference may be attributable to publication bias rather than intrinsic material advantages.

Overall, the current dataset does not provide convincing evidence that any particular 2D-material, device architecture, or switching mechanism intrinsically enables significantly higher on/off ratios. These observations underscore the need for more systematic and controlled studies that disentangle material properties from extrinsic factors such as device geometry, measurement protocols, and bias conditions. Only through such rigorously standardized assessments can the true potential of 2D-material memristors for delivering a sufficient dynamic range in practical in-memory computing systems be established.

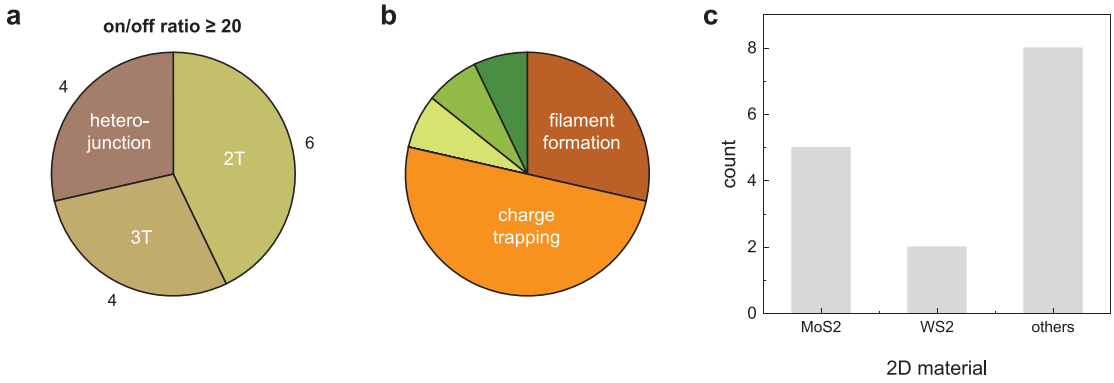


Figure 4. Analysis of 2D-material memristors with on/off ratios ⩾20. (a) Distribution by device structure, showing comparable representation of 2T, 3T, and heterojunction architectures. (b) Switching mechanisms contribute to high on/off ratios, dominated by filament formation and charge trapping. (c) Material distribution within this subset, with MoS_2 and WS_2 appearing most frequently, alongside other less common 2D materials.

4.3. Endurance

Endurance is a central performance metric for in-memory computing because analog weight updates must remain stable over billions of potentiation and depression cycles. Compared with the switching energy and on/off ratio, endurance data for 2D-material memristors are scarce and inconsistently reported. Many studies omit endurance testing, and when performed, the protocols often deviate from the pulse-driven analog switching conditions. This lack of a standardized evaluation hampers meaningful cross-comparisons across material platforms and device architectures.

Figure 5(a) shows the endurance distributions for the different device structures (2T, 3T, and heterojunctions). No systematic dependence was observed, as the interquartile ranges overlapped substantially. Similarly, figure 5(b) categorizes the endurance according to the switching mechanism, showing no strong correlation. Only a few outliers, most notably in the filament formation, demonstrated an endurance exceeding 10^7 cycles. To identify potential commonalities among higher-performing devices, we analyzed the subset with endurance $\geqslant 10^4$ (figures 5(c)–(e)). Among the 16 cases, hBN accounted for three cases, whereas MoS_2, WS_2, and SnS each contributed two cases (figure 5(c)). Although this distribution suggests a slight preference for hBN, the sample size was too small to be statistically significant. More informative patterns emerged when endurance was compared with other performance metrics. Figure 5(d) shows endurance versus E_{avg}. At approximately 10^4 cycles, E_{avg} spans a wide range; however, beyond this threshold, higher endurance generally coincides with a lower E_{avg}. The endurance was also compared with the average switching current and switching time (figure 5(e)). The switching current (blue points) shows no clear relationship with the endurance. By contrast, the switching time (yellow points) revealed a discernible trend: shorter switching times corresponded to longer endurance. This behavior suggests that rapid conductance modulation reduces the energy dissipation and mitigates long-term degradation.

Overall, the evidence suggests that minimizing switching time simultaneously reduces energy consumption and enhances endurance. High endurance has been consistently reported in devices dominated by filament formation, implying that this mechanism can benefit from rapid switching. Short switching times are likely to suppress thermally activated ion migration and unnecessary atomic rearrangements, thereby reducing the cumulative structural fatigue. This dynamic limits defect accumulation and stabilizes the conduction pathways over repeated cycling, enabling more reproducible weight updates.

4.4. Retention

Retention reflects the stability of conductance states over time and under specified thermal or bias conditions and is a critical determinant of long-term reliability in in-memory computing. However, as summarized in table 1, the retention of 2D-material memristors is typically limited to the 10^2–10^4 s range. Moreover, a large fraction of studies omits retention measurements entirely, and accelerated tests at elevated temperatures (85 °C or 125 °C) are almost absent. Consequently, demonstrations of the long-term stability of 2D systems are rare, leaving the reliability of analog switching insufficiently characterized in these devices. In addition, most reported retention studies do not capture the complete retention failure process. Instead, they generally demonstrate stable conductance only within a limited observation window, without identifying the onset of data loss or the ultimate retention limit. As a result, the reported

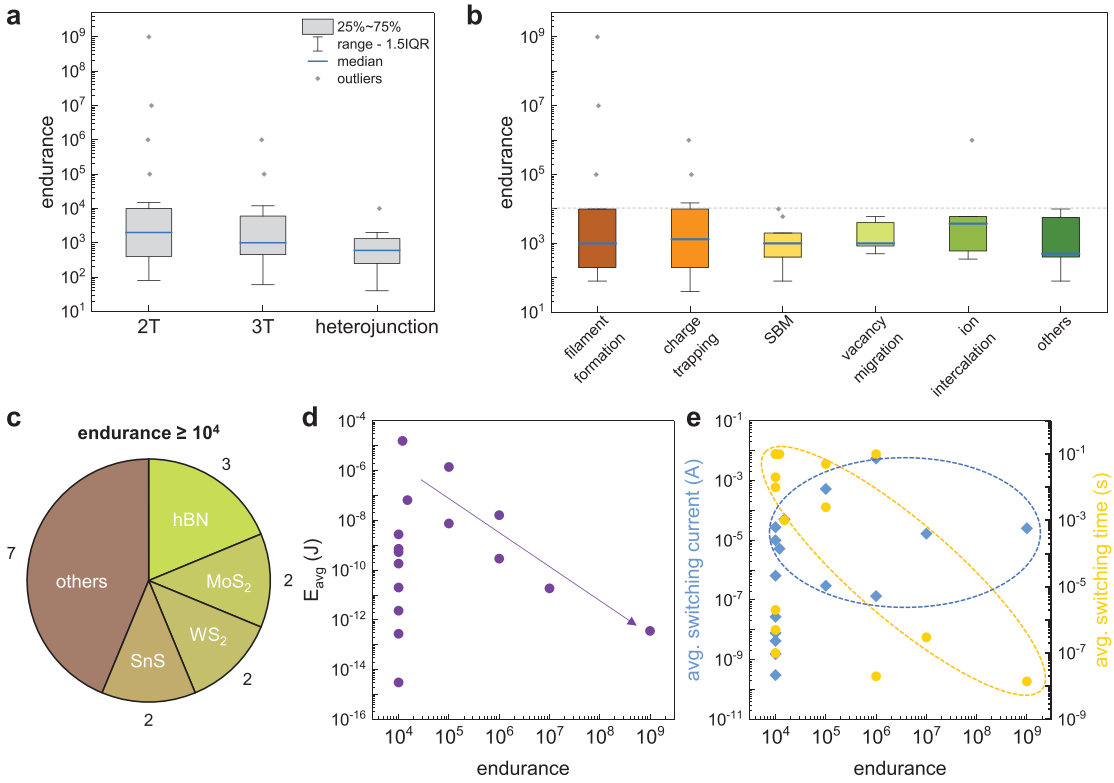


Figure 5. Endurance characteristics of 2D-material memristors. (a) Box plots of endurance values categorized by device structure (2T, 3T, and heterojunction). (b) Endurance distributions across switching mechanisms, with filament formation and charge trapping showing broad variability. (c) Material distribution among devices with endurance $\geqslant 10^4$ cycles, where hBN, MoS_2, WS_2, and SnS appear more frequently. (d) Correlation between endurance and E_{avg}, showing a trend toward lower energy consumption at higher endurance. (e) Endurance compared with average switching current (blue) and average switching time (yellow), indicating no clear relation with current but improved endurance with shorter switching times.

retention times often reflect the duration of the measurement rather than a fundamental stability ceiling of the device.

To obtain more reliable insights, we focused on devices exhibiting retentions longer than 10^4 s. This filtering criterion was adopted to enable a qualitative comparison among relatively stable devices, rather than to imply that shorter reported retention times represent intrinsic material limitations. Figure 6(a) shows that no particular device structure (2T, 3T, or heterojunction) confers a systematic advantage. A similar conclusion emerged when the dataset was categorized by switching mechanism (figure 6(b)); retention was distributed across filament formation, charge trapping, and vacancy migration, with no mechanism consistently associated with superior performance. When analyzed by material, MoS_2 (four cases) and graphene (two cases) appeared more frequently in the long retention subset. However, the small sample size prevents statistical significance, and the observed prevalence may simply reflect a reporting bias rather than intrinsic material benefits. Moreover, systematic studies examining the dependence of retention on measurement conditions (e.g. read bias, temperature, or stress protocol) or fabrication-related parameters such as defect density, interface quality, and material uniformity remain largely absent. Without such controlled investigations, it is difficult to decouple intrinsic physical processes from extrinsic process- and measurement-induced variability.

Overall, the available literature provides no compelling evidence that any specific material, device architecture, or switching mechanism inherently ensures enhanced retention in 2D-material memristors. Instead, retention remains an underexplored and insufficiently characterized performance metric. Addressing this gap will require systematic long-duration measurements, accelerated testing under elevated temperatures, and standardized evaluation protocols, complemented by targeted material and interface engineering strategies to stabilize conduction pathways over extended timescales.

4.5. Linearity

Linearity refers to the proportionality between the conductance modulation and the number of applied pulses. High linearity enables accurate estimation of the pulse count required to reach the target conductance, thereby facilitating precise weight mapping. Under such conditions, identical fixed-amplitude

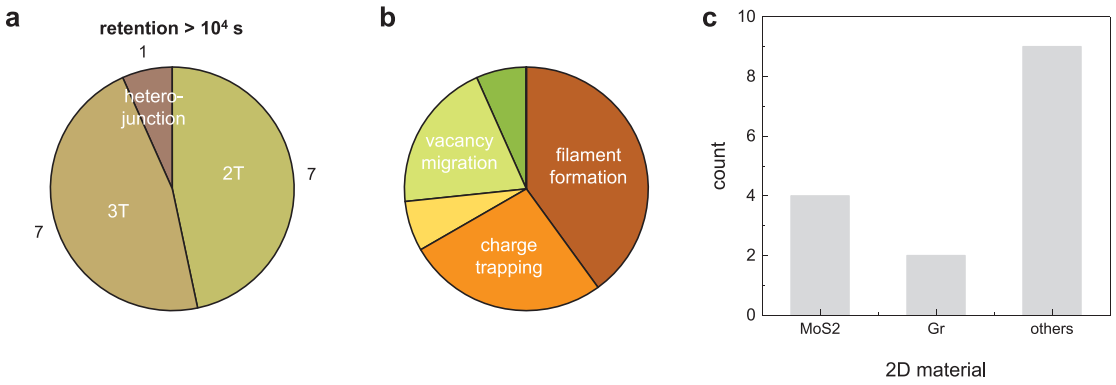


Figure 6. Retention characteristics of 2D-material memristors. (a) Distribution of devices with retention $>10^4$ s by structure, showing comparable representation of 2T and 3T architectures, with few heterojunction cases. (b) Associated switching mechanisms, including filament formation, charge trapping, and vacancy migration. (c) Material distribution within the long retention subset, where MoS_2 and graphene appear most frequently, alongside other 2D materials.

pulses can be employed to simplify the peripheral circuitry for weight update. However, in practice, the intrinsic switching mechanism of the resistive memory often introduces substantial nonlinearity. Threshold-driven processes, which are activated once a critical electric field or current density is exceeded, typically yield abrupt conductance jumps rather than gradual atomic-scale evolution. Consequently, many devices exhibit inherently nonlinear conductance updates. To address this challenge, circuit designers approximate the pulse–conductance relationship as a nonlinear function and dynamically adjust the pulse number or characteristics. Although effective, this strategy increases circuit complexity and energy consumption, motivating extensive efforts to achieve more linear responses. Several circuit- and protocol-level approaches were also explored. A widely used method is current limitation, which is achieved either through compliance current control or transistor gating to suppress abrupt conductance changes. Variable pulse schemes, in which the amplitude or duration is progressively tuned, are another common strategy. Alternatively, closed-loop write–verify protocols apply a pulse, measure the resulting conductance, and iteratively adjust the subsequent pulses.

Within the dataset summarized in table 1, studies marked with 'O' in the linearity column employed variable pulse schemes to improve linearity. In 2D-material memristors, progress to date has relied almost exclusively on adaptive pulsing, with no reports of alternative circuit- or protocol-level strategies commonly applied to other memristor platforms. Because the improved linearity in these cases arises from external control rather than from intrinsic device characteristics, direct cross-device comparisons are difficult. To avoid this complication, we focused on devices operating under fixed-amplitude pulse trains without adaptive schemes. Among these, devices exhibiting comparatively improved linearity were selectively annotated as '△'. Unlike other memristor platforms, where linearity is often quantified using the nonlinearity factor (NL) and is systematically benchmarked, 2D-material studies rarely report explicit NL values, precluding rigorous comparisons. Thus, the '△' classification represents a qualitative selection based on literature descriptions. While provisional and intended as a heuristic classification, this approach highlights devices with intrinsically superior linearity and underscores the urgent need for standardized quantitative metrics.

A comparison between the '△' and 'non-△' cases reveals several clear patterns. As shown in figure 7(a), nearly all favorable cases adopted a three-terminal (3T) architecture, underscoring the importance of the gate electrode in enabling gradual conductance modulation. Furthermore, these devices predominantly exploit the charge-trapping, SBM, and ion-intercalation mechanisms (figure 7(b)). This contrasts with other performance metrics such as energy efficiency or endurance, where filamentary switching is often advantageous. However, filamentary processes are inherently detrimental to linearity because of their abrupt, threshold-driven transitions. Collectively, these observations indicate that gate-controlled mechanisms that facilitate conductance changes through trapping, Schottky barrier tuning, or ionic redistribution are better suited for proportional weight updates than filamentary conduction. Figure 7(c) further categorizes the '△' cases by material, with MoS_2 and WSe_2 appearing most frequently. Although the small size of the dataset precluded statistical significance, its prevalence may reflect experimental popularity rather than intrinsic superiority.

The potential correlations with other metrics are shown in figures 7(d) and (e). As shown in figure 7(d), both E_{avg} and on/off ratio overlap substantially between '△' and 'non-△' cases, indicating

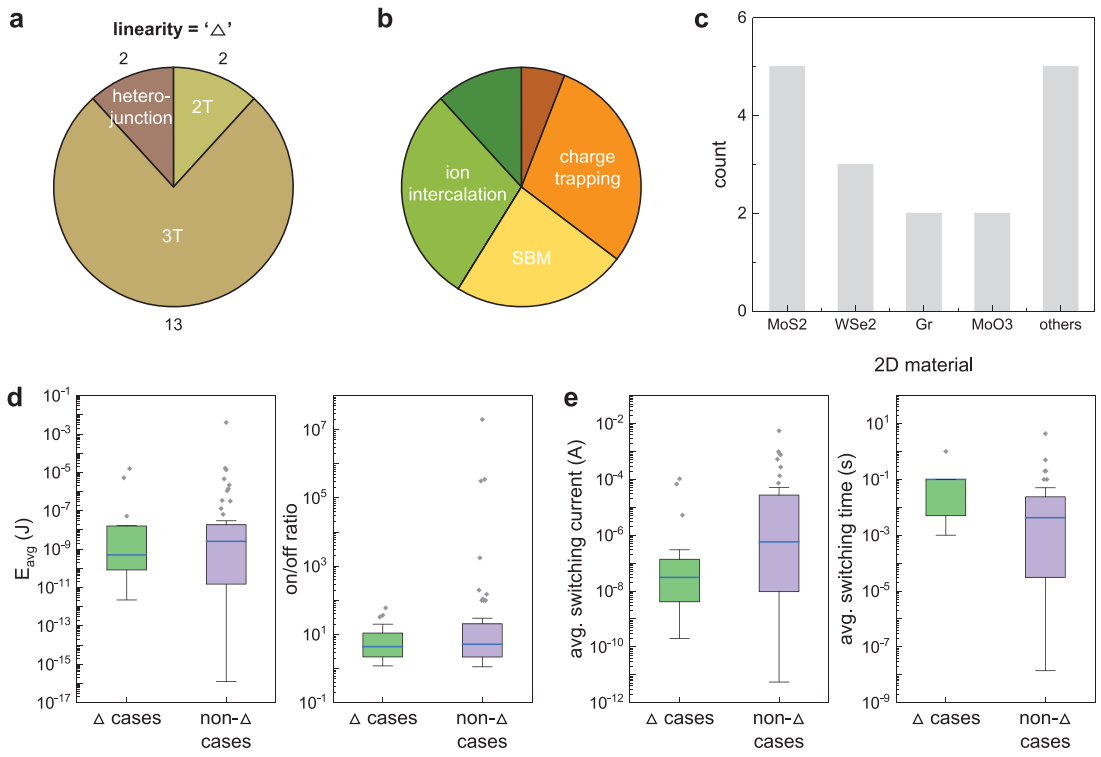


Figure 7. Linearity characteristics of 2D-material memristors. (a) Device structure distribution of cases with improved linearity ('△'), showing strong prevalence of 3T architectures. (b) Associated switching mechanisms, dominated by charge trapping, SBM, and ion intercalation. (c) Material distribution of linearity-enhanced devices, with MoS_2 and WSe_2 appearing most frequently. (d) Comparison of E_{avg} and on/off ratio between △ and non-△ cases, showing no clear dependence on these parameters. (e) Comparison of average switching current and switching time, indicating that △ cases generally operate at lower current levels and longer switching times, consistent with gradual conductance modulation.

no clear dependence of linearity on these parameters once outliers are excluded. By contrast, figure 7(e) reveals consistent trends: devices with superior linearity operate at lower switching currents and longer switching times. This suggests that gradual conductance modulation requires slow low-current transitions, in contrast to the abrupt high-current behavior of filamentary switching. Therefore, mechanisms that enable continuous field-driven conductance evolution, such as charge trapping, SBM, and ion intercalation, are intrinsically favorable. The additional electrostatic control provided by the gate electrode in the 3T architecture further suppresses abrupt transitions and promotes incremental updates.

Overall, the analysis established that linear conductance modulation in 2D-material memristors is predominantly realized in 3T architectures employing gate-controlled mechanisms such as charge trapping, SBM, and ion intercalation. Superior linearity is consistently associated with reduced switching current levels; however, achieving a sufficient dynamic range requires longer switching times. This indicates an inherent trade-off between linearity and switching speed. Although the current evidence remains limited and largely qualitative, these observations highlight both the promise of gate-controlled strategies and the urgent need for standardized quantitative benchmarks to enable rigorous cross-platform evaluation.

5. Discussion

5.1. Device-level interpretation of analog switching metrics

Our comparative analysis demonstrates that no single device category or switching mechanism offers a universal advantage; instead, performance is defined by competing trade-offs. Ultrafast filamentary switching in ultrathin 2T devices minimizes energy consumption and improves endurance but inevitably compromises linearity owing to abrupt, threshold-driven transitions. Conversely, 3T gate-controlled architectures that exploit charge trapping, SBM, or ion intercalation enable gradual conductance evolution and superior linearity but only at the expense of extended switching times. Similarly, inflated on/off

ratios often arise from the artificial suppression of the minimum conductance state, undermining the dynamic range and readout reliability. These trends highlight that optimizing one metric frequently degrades another, underscoring the need for designs that balance multiple figures of merit rather than maximize a single attribute.

The data further indicate that the intrinsic attributes of 2D-materials, such as atomic-scale thickness, dangling-bond-free surfaces, and van der Waals interfaces, do not uniformly translate into superior device performance. Their benefits emerge selectively: ultrathin channels confine ionic transport to reduce switching energy, whereas interfacial traps in heterostructures provide gate tunability for analog conductance control. However, these gains remain constrained by extrinsic factors, such as fabrication variability, inconsistent measurement protocols, and limited CMOS compatibility. Compared with oxide-based platforms, 2D-material memristors continue to lag in endurance, retention, and reproducibility, although they offer unique prospects for ultralow-power operation, flexible integration, and unconventional form factors.

Realizing this potential requires coordinated progress across multiple fronts. Standardized benchmarking of pulsed on/off ratios, endurance under analog operation, and high-temperature retention is crucial for establishing reliable cross-platform comparisons. Advances in scalable CVD growth coupled with defect engineering and controlled heterojunction formation are necessary to reduce variability and improve integration. At the device–circuit interface, multi-terminal architectures and co-optimized programming schemes may help reconcile the trade-offs between linearity and speed and between energy and endurance. Ultimately, the future role of 2D-materials in in-memory computing will be determined not by isolated device demonstrations but by their capacity to deliver reproducible, system-level advantages under rigorous and standardized evaluation.

5.2. System-level implications for analog in-memory computing

Taken together, these observations indicate that linearity, endurance, and retention must be interpreted from a system-level perspective. Ideally, a perfectly linear relationship between the number of identical programming pulses and the resulting conductance change would be desirable, as it would simplify weight updates and minimize computational error. However, achieving such intrinsic linearity in 2D-material memristors remains challenging due to threshold-driven switching and defect-mediated transport processes. In practice, high-precision analog weight updates can nevertheless be realized using closed-loop write–verify schemes, which effectively compensate for intrinsic nonlinearity and are therefore well suited for accuracy-critical operations such as on-chip training. When the overhead associated with write–verify control is prohibitive in terms of latency, energy, or circuit complexity, restricting the number of available conductance states through appropriate quantization offers an alternative strategy to mitigate nonlinearity-induced errors, particularly for inference-oriented workloads.

Similar system-dependent considerations apply to endurance and retention. During training, conductance states are frequently updated, placing stringent demands on endurance. In contrast, during inference, conductance states are largely static, making long-term stability and retention the dominant reliability concern. Although universal benchmarks for endurance and retention in 2D-material memristors are difficult to define at present, performance targets comparable to those of commercial single-level cell flash memory—namely endurance exceeding 10^6 cycles and retention times on the order of 10 years—provide a useful order-of-magnitude reference for assessing the long-term practical viability of these devices in analog in-memory computing systems.

Beyond these metrics, D2D and C2C variability constitutes an equally critical system-level constraint. In large crossbar arrays, even modest variability can accumulate across devices, degrading training efficiency and inference accuracy. However, quantitative analysis of D2D and C2C variability is currently hindered by the state of the literature. Most studies report single-device results or a limited number of representative curves without explicit statistical descriptors such as device count, standard deviation, or distribution data. Moreover, definitions and measurement protocols for variability differ widely across reports, rendering direct cross-study comparison statistically and physically unjustified. Accordingly, this review refrains from performing a quantitative variability comparison and instead identifies variability as a critical yet insufficiently characterized bottleneck for translating 2D-material memristors from single-device demonstrations to realistic array-level implementations. Systematic multi-device studies with standardized variability metrics under pulse-driven operating conditions will be essential to enable rigorous system-level assessment.

5.3. Implications of fabrication methods: exfoliation versus CVD

Fabrication method is often considered a key factor governing scalability, uniformity, and device performance. In 2D-material memristors, mechanical exfoliation and CVD dominate the reported literature, as shown in figure 2(b). Exfoliation is typically associated with high crystalline quality and clean interfaces, favoring fundamental and proof-of-concept studies, whereas CVD offers clear advantages in wafer-scale growth and integration compatibility.

Despite these expectations, our analysis reveals no consistent correlation between fabrication method and key analog switching metrics, including switching energy, on/off ratio, endurance, retention, or the demonstration of array-level operation. Devices fabricated by exfoliation and CVD exhibit broadly overlapping performance distributions across all examined metrics. Notably, this lack of correlation persists even for array-based demonstrations, where CVD would intuitively be expected to dominate. Instead, a substantial fraction of reported array-level studies relies on exfoliated 2D materials. These observations indicate that, at the current stage of the field, analog switching behavior is governed more strongly by switching mechanism, interface quality, and local defect configurations than by the macroscopic fabrication route. Exfoliated materials remain attractive because they provide superior control over material quality and interfacial cleanliness, which are critical for stabilizing analog conductance modulation. Conversely, the potential scalability advantages of CVD have not yet translated into systematically improved memristor performance, likely due to additional variability introduced by grain boundaries and process-dependent defects.

Overall, the present literature does not support a definitive performance or integration advantage associated with either exfoliation or CVD. Rather, this absence of clear trends reflects the early and exploratory nature of 2D-material memristor research and underscores the need for future studies that directly compare fabrication methods under controlled and standardized conditions.

5.4. Device area and scalability considerations

Device area is a key determinant of integration density, die size, and cost in resistive crossbar arrays, where practical analog in-memory computing hardware requires scaling individual memory cells to lateral dimensions on the order of tens of nanometers. In contrast, nearly all experimentally reported 2D-material memristors operate at micrometer-scale device areas, as summarized in table 1. At this scale, device dimensions are largely dictated by experimental constraints, such as flake size, lithographic convenience, and probing accessibility, rather than by density-optimized design rules relevant to large-scale crossbar integration.

As a result, the current literature does not yet provide a meaningful basis for evaluating the scalability of 2D-material memristors in terms of cell footprint, die size, or cost. The absence of demonstrations at technologically relevant nanometer-scale dimensions precludes quantitative comparison with mature oxide-based memristor technologies. Existing studies should therefore be interpreted primarily as proof-of-concept demonstrations that establish feasible switching mechanisms and analog modulation behavior, rather than as validations of scalable device architectures. Future progress will require explicit targeting of nanometer-scale patterning, dense array integration, and parasitic-aware operation before the scalability and practical competitiveness of 2D-material memristors can be rigorously assessed.

5.5. Status and limitations of application-level demonstrations

Recent studies increasingly report application-oriented demonstrations of 2D-material memristors for analog in-memory computing. Across a broad range of 2D materials, many recent works exploit analog resistive switching to emulate synaptic weight updates and to evaluate neural-network inference tasks, most commonly using benchmark datasets such as MNIST (Modified National Institute of Standards and Technology). These results collectively indicate that 2D-material memristors can, in principle, support multilevel conductance modulation suitable for analog weight representation.

However, a closer examination reveals that the vast majority of these demonstrations rely on a highly idealized and indirect evaluation framework. Typically, analog switching characteristics are first extracted from single devices and described using phenomenological models that relate the number of programming pulses to conductance change. It is then assumed that memristors with identical characteristics form a crossbar array, which is mapped onto a simplified neural-network architecture. In this approach, memristors function as synaptic weight elements, and inference accuracy is assessed exclusively through circuit- or system-level simulations rather than through experimentally fabricated arrays.

This methodology imposes fundamental limitations on the interpretation of application-level results. D2D and C2C variations are generally neglected, leading to simulations that assume uniform and time-invariant device behavior. Moreover, the quantitative relationship between specific analog switching metrics—such as linearity, asymmetry, dynamic range, and noise—and recognition accuracy is

rarely analyzed in a systematic manner. As a result, existing studies should be interpreted primarily as proof-of-concept demonstrations of feasibility, rather than as rigorous validations of practical and scalable analog in-memory computing hardware. Progress toward realistic implementations will require experimentally validated array-level demonstrations that explicitly incorporate device variability and establish clear, quantitative links between device-level switching metrics and system-level performance.

6. Conclusions

Our comparative analysis shows that 2D-material memristors occupy distinct, mechanism-defined operating regimes rather than a single, universally superior performance envelope. Ultrafast filamentary switching in ultrathin two-terminal stacks minimize energy and can support high endurance; however, it intrinsically compromises linearity. By contrast, gate-controlled three-terminal architectures achieve the most proportional weight updates through charge trapping, SBM, or ion intercalation, albeit at lower currents over longer timescales. The observation that higher linearity correlates with reduced switching currents suggests that low-current operation is inherently favorable for proportional conductance updates. However, securing a sufficient dynamic range under such conditions appears to require unavoidably long switching times, thereby establishing a fundamental trade-off between linearity and switching speed. The reported dynamic on/off ratios and high-temperature retention remain limited, and the DC sweep inflation continues to obscure the true analog operating window. Consequently, the atomic thickness and van der Waals interfaces of 2D-materials provide selective advantages rather than universal dominance.

These findings highlight three key priorities for advancing the field. First, establish rigorous, interoperable metrics focused on pulsed operation, including dynamic on/off, write-verify-free linearity, endurance under analog cycling, and accelerated retention at 85 °C–125 °C. Second, close the variability gap through scalable growth and interface engineering, particularly CVD with controlled defect densities and reproducible heterojunction formation, to reconcile D2D dispersion with array-level accuracy. Third, co-optimize devices and programming schemes: exploit ultrathin two-terminal stacks, where energy and endurance dominate, and deploy three-terminal gate-assisted updates, where linearity and precision are paramount. Ultimately, the practical role of 2D-materials in in-memory computing will be determined by reproducible system-level demonstrations under standardized testing rather than isolated device benchmarks.

The scope of this review was intentionally limited to memristive devices in which the active switching layer consists exclusively of 2D materials. This restriction reflects the current state of the literature, where even nominally similar 2D-material memristors exhibit substantial variability in switching mechanisms and performance trade-offs that have yet to be systematically reconciled across material systems. Inclusion of hybrid architectures—such as 2D-material/oxide or 2D-material/polymer heterojunctions—would introduce additional variables associated with interfacial chemistry, band alignment, and extrinsic defect contributions, thereby complicating cross-platform statistical comparison. Nevertheless, hybrid heterojunction systems offer a promising route to overcoming several limitations identified for purely 2D-material memristors, particularly with respect to endurance, retention, and CMOS compatibility. In practical hardware implementations, 2D materials are therefore more likely to complement, rather than directly compete with, mature oxide- or polymer-based analog devices by functioning as ultrathin active layers, interfacial modifiers, or gate-tunable elements within hybrid stacks. Systematic investigation of such hybrid integration strategies—especially under back-end-of-line-compatible thermal budgets—represents an important direction for future research building upon the present review.

Acknowledgment

This work was supported by National Research Foundation of Korea (NRF) grants funded by the Korean government (MSIT and MOE) (RS-2024-00449412, RS-2025-16063688).

Data availability statement

No new data were created or analyzed in this study.

Conflict of interest

The authors declare no competing interests.

Author contributions

Jimin Shim
Data curation (equal), Investigation (equal)

Jayoung Yoon
Data curation (equal), Investigation (equal)

Sookyung Shin
Data curation (equal), Investigation (equal)

Eunsu Hwang
Data curation (equal), Investigation (equal)

Dokyoung Lee 0009-0007-3590-1414
Validation (equal), Visualization (equal)

Moon-Seok Kim
Resources (equal), Validation (equal)

Sungho Kim 0000-0002-7004-3482
Supervision (equal), Writing – original draft (equal), Writing – review & editing (equal)

References

[1] Akarvardar K and Wong H S P 2023 *Proc. IEEE* **111** 92–112
[2] Oh K S and Jung K 2004 *Pattern Recognit.* **37** 1311–4
[3] Nair R 2015 *Proc. IEEE* **103** 1331–45
[4] Ielmini D and Wong H S P 2018 *Nat. Electron.* **1** 333–43
[5] Haensch W, Gokmen T and Puri R 2019 *Proc. IEEE* **107** 108–22
[6] Verma N, Jia H, Valavi H, Tang Y, Ozatay M, Chen L Y, Zhang B and Deaville P 2019 *IEEE Solid-State Circ. Mag.* **11** 43–55
[7] Jung S *et al* 2022 *Nature* **601** 211–6
[8] Li C *et al* 2018 *Nat. Electron.* **1** 52–59
[9] Zhong Y *et al* 2022 *Nat. Electron.* **5** 672–81
[10] Bengel C, Zhang K, Mohr J, Ziegler T, Wiefels S, Waser R, Wouters D and Menzel S 2023 *Front. Electron. Mater.* **3** 1061269
[11] Kim S, Kim H and Choi S 2019 *Sci. Rep.* **9** 15237
[12] Roldán J B *et al* 2023 *Adv. Intell. Syst.* **5** 2200338
[13] Asif M and Kumar A 2022 *Mater. Today Electron.* **1** 100004
[14] Yao P, Wu H, Gao B, Tang J, Zhang Q, Zhang W, Yang J J and Qian H 2020 *Nature* **577** 641–6
[15] Li C *et al* 2018 *Nat. Commun.* **9** 2385
[16] Zhang W, Gao B, Tang J, Yao P, Yu S, Chang M F, Yoo H J, Qian H and Wu H 2020 *Nat. Electron.* **3** 371–82
[17] Duong D L, Yun S J and Lee Y H 2017 *ACS Nano* **11** 11803–30
[18] Wang X, Song Z, Wen W, Liu H, Wu J, Dang C, Hossain M, Ahsan Iqbal M and Xie L 2019 *Adv. Mater.* **31** 1804682
[19] Zhou H, Li S, Ang K W and Zhang Y W 2024 *Nanomicro Lett.* **16** 121
[20] Kim M and Kim S 2024 *ACS Appl. Electron. Mater.* **6** 3998–4015
[21] Li D, Wu B, Zhu X, Wang J, Ryu B, Lu W D, Lu W and Liang X 2018 *ACS Nano* **12** 9240–52
[22] Sangwan V K, Lee H S, Bergeron H, Balla I, Beck M E, Chen K S and Hersam M C 2018 *Nature* **554** 500–4
[23] Bao L *et al* 2019 *ACS Appl. Mater. Interfaces* **11** 41482–9
[24] Wang L *et al* 2019 *Adv. Funct. Mater.* **29** 1901106
[25] Xu R, Jang H, Lee M H, Amanov D, Cho Y, Kim H, Park S, Shin H J and Ham D 2019 *Nano Lett.* **19** 2411–7
[26] Zhu X, Li D, Liang X and Lu W D 2019 *Nat. Mater.* **18** 141–8
[27] Lee H S, Sangwan V K, Rojas W A G, Bergeron H, Jeong H Y, Yuan J, Su K and Hersam M C 2020 *Adv. Funct. Mater.* **30** 2003683
[28] Ranganathan K, Fiegenbaum-Raz M and Ismach A 2020 *Adv. Funct. Mater.* **30** 2005718
[29] Li D, Ryu B, Yoon J, Li Z and Liang X 2020 *J. Phys. D: Appl. Phys.* **53** 135305
[30] Feng X, Li S, Wong S L, Tong S, Chen L, Zhang P, Wang L, Fong X, Chi D and Ang K W 2021 *ACS Nano* **15** 1764–74
[31] Song Y W, Song M K, Choi D and Kwon J Y 2021 *J. Alloys Compd.* **885** 161016
[32] Yuan J *et al* 2021 *Nano Lett.* **21** 6432–40
[33] Zhang L *et al* 2022 *Adv. Mater. Interfaces* **9** 2201775
[34] Tang B *et al* 2022 *Nat. Commun.* **13** 3037
[35] Jang H Y, Kwon O, Nam J H, Kwon J D, Kim Y, Park W and Cho B 2022 *ACS Appl. Mater. Interfaces* **14** 52173–81
[36] Naqi M, Kang M S, Liu N, Kim T, Baek S, Bala A, Moon C, Park J and Kim S 2022 *npj 2D Mater. Appl.* **6** 53
[37] Lee E, Kim J, Park J, Hwang J, Jang H, Cho K and Choi W 2023 *ACS Appl. Mater. Interfaces* **15** 15839–47
[38] Xiong X, Wu F, Ouyang Y, Liu Y, Wang Z, Tian H and Dong M 2024 *Adv. Funct. Mater.* **34** 2213348

[39] Fu S, Park J H, Gao H, Zhang T, Ji X, Fu T, Sun L, Kong J and Yao J 2023 *Nano Lett.* **23** 5869–76
[40] Lee Y *et al* 2024 *ACS Nano* **18** 14327–38
[41] Spetzler B, Sangwan V K, Hersam M C and Ziegler M 2025 *npj 2D Mater. Appl.* **9** 1–14
[42] Xie J, Afshari S and Sanchez Esqueda I 2022 *npj 2D Mater. Appl.* **6** 1–7
[43] Song J, Moon S, Byun J, Kim J, Choi J, Kwak H, Hwang I, Ji C, Kim S and Kim J K 2025 *Small* **21** 2504507
[44] Afshari S, Radhakrishnan S, Xie J, Musisi-Nkambwe M, Meng J, He W, Seo J S and Sanchez Esqueda I 2023 *2D Mater.* **10** 035031
[45] Afshari S, Xie J, Musisi-Nkambwe M, Radhakrishnan S and Sanchez Esqueda I 2023 *Nanotechnology* **34** 445703
[46] Zhang H *et al* 2024 *Chem. Eng. J.* **498** 155651
[47] Kim J *et al* 2024 *Small* **20** 2403737
[48] Ahn W, Lee S, Oh J, Lee H and Choi S Y 2025 *Adv. Mater.* **37** 2413640
[49] Jo Y, Noh G, Park E, Lee D K, Jeong Y J, Wi H and Kwak J Y 2024 *Chaos Solitons Fractals* **187** 115390
[50] Zhu J *et al* 2018 *Adv. Mater.* **30** 1800195
[51] Luo S *et al* 2021 *Nanoscale* **13** 6654–60
[52] Ding G, Yang B, Chen R-S, Mo W-A, Zhou K, Liu Y, Shang G, Zhai Y, Han S-T and Zhou Y 2021 *Small* **17** 2103175
[53] Ren J, Shen H, Liu Z, Xu M and Li D 2022 *ACS Appl. Mater. Interfaces* **14** 21141–9
[54] Leong J F, Fang Z, Sivan M, Pan J, Tang B, Zamburg E and Thean A V Y 2023 *Adv. Funct. Mater.* **33** 2302949
[55] Yan X *et al* 2019 *ACS Appl. Mater. Interfaces* **11** 48029–38
[56] Kumar M, Ban D K, Kim S M, Kim J and Wong C P 2019 *Adv. Electron. Mater.* **5** 1900467
[57] Rasouli H R, Kim J, Mehmood N, Sheraz A, Jo M K, Song S, Kang K and Kasirga T S 2021 *Nano Lett.* **21** 3997–4005
[58] Ji Y, Wang L, Long Y, Wang J, Zheng H, Yu Z G, Zhang Y W and Ang K W 2025 *Nat. Commun.* **16** 1–12
[59] Li B, Li S, Wang H, Chen L, Liu L, Feng X, Li Y, Chen J, Gong X and Ang K W 2020 *Adv. Electron. Mater.* **6** 2000760
[60] Lu Z, Li D, Chen E, Li W, Liu T, Zhang M, Zheng X, Wang X, Wan X and Chen K 2025 *ACS Appl. Nano Mater.* **8** 9016–24
[61] Sharbati M T, Du Y, Torres J, Ardolino N D, Yun M and Xiong F 2018 *Adv. Mater.* **30** 1802353
[62] Chen Y, Zhou Y, Zhuge F, Tian B, Yan M, Li Y, He Y and Miao X S 2019 *npj 2D Mater. Appl.* **3** 31
[63] Yu C *et al* 2024 *Nano Lett.* **24** 1620–8
[64] Vu T T H *et al* 2025 *Appl. Surf. Sci.* **689** 162460
[65] Wang Y, Huang Y, Fan S, Lu H and Liu J 2025 *Chem. Eng. J.* **513** 163079
[66] Xiang D, Liu T, Zhang X, Zhou P and Chen W 2021 *Nano Lett.* **21** 3557–65
[67] Li Y, Loh L, Li S, Chen L, Li B, Bosman M and Ang K W 2021 *Nat. Electron.* **4** 348–56
[68] Li S, Li B, Feng X, Chen L, Li Y, Huang L, Fong X and Ang K W 2021 *npj 2D Mater. Appl.* **5** 1–10
[69] Pam M E, Li S, Su T, Chien Y C, Li Y, Ang Y S and Ang K W 2022 *Adv. Mater.* **34** 2202722
[70] Kwon K C *et al* 2020 *ACS Nano* **14** 7628–38
[71] Lu X F *et al* 2021 *Nano Lett.* **21** 8800–7
[72] Jang E K, Park Y and Lee J S 2019 *Nanoscale* **11** 15382–8
[73] Rehman S, Khan M F, Kim H-D and Kim S 2022 *Nat. Commun.* **13** 1–8
[74] Yan X *et al* 2019 *Small* **15** 1900107
[75] Yang C S, Shang D S, Liu N, Shi G, Shen X, Yu R C, Li Y Q and Sun Y 2017 *Adv. Mater.* **29** 1700906
[76] Yang C-S, Shang D-S, Liu N, Fuller E J, Agrawal S, Talin A A, Li Y-Q, Shen B-G and Sun Y 2018 *Adv. Funct. Mater.* **28** 1804170
[77] Huang C H, Chang H, Yang T Y, Wang Y C, Chueh Y L and Nomura K 2021 *ACS Appl. Mater. Interfaces* **13** 52822–32
[78] Tian H, Guo Q, Xie Y, Zhao H, Li C, Cha J J, Xia F and Wang H 2016 *Adv. Mater.* **28** 4991–7
[79] Tian H *et al* 2017 *ACS Nano* **11** 7156–63
[80] Yi S G, Park M U, Kim S H, Lee C J, Kwon J, Lee G H and Yoo K H 2018 *ACS Appl. Mater. Interfaces* **10** 31480–7
[81] Huh W *et al* 2018 *Adv. Mater.* **30** 1801447
[82] Seo S *et al* 2018 *Nat. Commun.* **9** 1–8
[83] He C *et al* 2020 *ACS Appl. Mater. Interfaces* **12** 11945–54
[84] Park S *et al* 2020 *ACS Nano* **14** 12064–71
[85] Nam J H, Oh S, Jang H Y, Kwon O, Park H, Park W, Kwon J-D, Kim Y and Cho B 2021 *Adv. Funct. Mater.* **31** 2104174
[86] Wang S, Liu L, Gan L, Chen H, Hou X, Ding Y, Ma S, Zhang D W and Zhou P 2021 *Nat. Commun.* **12** 1–9
[87] Li Y, Chen S, Yu Z, Pam M-E, Zhang Y-W and Ang K-W 2022 *Adv. Mater.* **34** 2201488
[88] Huh W *et al* 2023 *Adv. Mater.* **35** 2211525
[89] Won U Y *et al* 2023 *Nat. Commun.* **14** 1–11
[90] Wang X, Chen F, Li X, Xiang T and Wang L 2024 *ACS Appl. Electron. Mater.* **6** 4311–20
[91] Sun L *et al* 2025 *Nano Energy* **143** 111311
[92] Ma X, Zhou Y, Li R, Zhao S and Zhang M 2025 *ACS Appl. Mater. Interfaces* **17** 18582–91