Check for updates

Electronics Letters

LETTER OPEN ACCESS

A High Temperature–Voltage Sensitivity 2-Transistor Voltage Reference With Wide Range Operation

Myung-Hyun Jeon[1] | Yeonsu Kim[1] | Hyunyoung Yoo[1] | Eunji Yoo[1] | Jusung Kim[2] | Min-Woo Kwon[1] | Jae-Won Nam[1]

[1]Department of Electronic Engineering, Seoul National University of Science and Technology, Seoul, Republic of Korea | [2]Division of Electronic and Semiconductor Engineering and with the Institute for Multiscale Matter and Systems (IMMS) Laboratory, Ewha Womans University, Seoul, Republic of Korea

Correspondence: Min-Woo Kwon (mwkwon@seoultech.ac.kr) | Jae-Won Nam (jaewon.nam@seoultech.ac.kr)

Received: 23 November 2025 | **Revised:** 21 January 2026 | **Accepted:** 2 February 2026

ABSTRACT

Measurement of the temperature in an integrated circuit (IC) is essential for evaluating temperature-dependent circuit performance. Using off-chip temperature sensors for this purpose has limited accuracy in sensing the on-chip temperature. For on-chip integration with ICs, a low-power and compact temperature sensor is required. Therefore, this letter presents a 2-Transistor (2T) voltage reference generator (VRG) that overcomes the limited sensitivity of conventional structures through the deep-subthreshold operation and achieves high T–V sensitivity by employing the narrow-width effect. The proposed 2T VRGs are implemented in 28-nm FD-SOI process and demonstrated to operate over a temperature range of 200 to 400 K, achieving a 0.86 mV/K T–V sensitivity with 3.6% relative inaccuracy.

1 | Introduction

On-chip thermal management is required for readout integrated circuits (ROICs) that are highly sensitive to thermal noise. In most cases, the temperature of the ICs is monitored using temperature sensors mounted on the chamber or PCB [1–3]. However, the thermal impedance between the external environment and the chip disrupts the accurate sensing of the on-chip temperature [1]. To obtain a true on-chip temperature, the integration of the on-chip temperature sensors is essential. In CMOS technology, bipolar junction Transistor (BJT)-based transducers, which convert on-chip temperature into an analogue signal, are the most widely used in temperature sensors [4–9]. However, the large area and high power consumption restrict the implementation of large-array temperature sensors for ROIC thermal management [10].

A common approach to designing CMOS-based temperature transducers for temperature sensors is to exploit the temperature dependence of the MOSFET subthreshold current [10–13]. In a prior study [10], the 2-Transistor (2T) proportional to absolute temperature (PTAT) voltage reference generator (VRG) is proposed. Owing to its compact size, picowatt-level power consumption and inherent linearity, the 2T PTAT VRG is suitable for the implementation of an on-chip temperature sensor for ROIC thermal management. However, the low temperature–voltage (T–V) sensitivity poses a challenge in using the architecture as a temperature transducer for temperature sensors.

Several studies have improved the T–V sensitivity by reconfiguring the conventional 2T PTAT VRG. Reference [14] achieves a 0.27 mV/K T–V sensitivity by modifying the conventional structure, and reference [11] proposes the 3-Transistor (3T) PTAT VRG with a 0.37 mV/K T–V sensitivity. In [12], the T–V comparator is proposed with a 0.48 mV/K T–V sensitivity, and [13] achieves a 0.98 mV/K T–V sensitivity by combining the T–V comparator and the 2T PTAT VRG proposed in [14]. However, compared

Myung-Hyun Jeon and Yeonsu Kim contributed equally to this work.

This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

© 2026 The Author(s). *Electronics Letters* published by John Wiley & Sons Ltd on behalf of The Institution of Engineering and Technology.

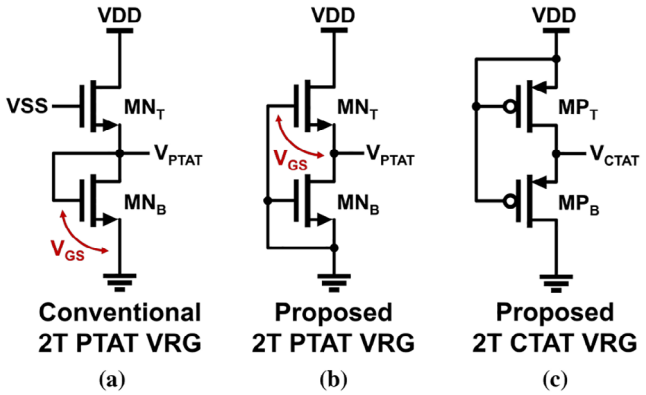


FIGURE 1 | (a) Conventional 2T PTAT VRG proposed in [14]. (b) Proposed 2T PTAT VRG and (c) proposed 2T CTAT VRG.

to 2T VRG, the T–V comparator requires more transistors due to its differential architecture, which requires more area and power consumption. Therefore, this letter proposes a 2T VRG with a high T–V sensitivity. The proposed 2T VRG overcomes the limitation of the conventional structures in achieving high T–V sensitivity. Moreover, the PMOS-based 2T complementary to absolute temperature (CTAT) VRG resolves the fundamental low sensitivity issue of the conventional NMOS-based 2T VRGs by employing the narrow-width effect (NWE). The proposed 2T VRGs are fabricated in 28-nm fully depleted silicon on insulator (FD-SOI) process and validated by measurement results.

2 | Proposed 2T PTAT VRG

Figure 1a,b illustrates the conventional and proposed 2T PTAT VRGs. For the drain-to-source voltage above $5V_T$, the output voltage of both the conventional and proposed structures, derived from the subthreshold current [15, 16] including the body and DIBL effect, is given as follows:

$$V_{PTAT} = \frac{1}{1+\eta_T+\eta_B+\gamma_T} \cdot \left\{ mV_T \cdot \ln \frac{W_T L_B}{L_T W_B} + \eta_T V_{DD} + (V_{TH.B} - V_{TH.T}) \right\}. \quad (1)$$

As shown in Equation (1), 2T VRG can obtain a high T–V sensitivity by adjusting the stacked-MOSFETs size ratio. However, a higher sensitivity results in a higher V_{PTAT}, which derives the MN_B in the conventional structure into the saturation region where the temperature-linear analytic solution is no longer valid. In contrast, the proposed structure connects the transistor gates to ground, and thus the analytical solution remains valid even at large size ratios.

Figures 2 and 3 show the simulation results of the conventional and proposed 2T PTAT VRGs using 28-nm FD-SOI process. Figure 2a illustrates $V_{GS} - V_{TH}$ as a function of size ratio, and Figure 2b presents T–V sensitivity as a function of size ratio. In small size ratios, both the conventional and proposed structures follow the subthreshold current-based analytical solution. However, when the size ratio exceeds 256, MN_B in the conventional structure enters the saturation region. In the case of proposed

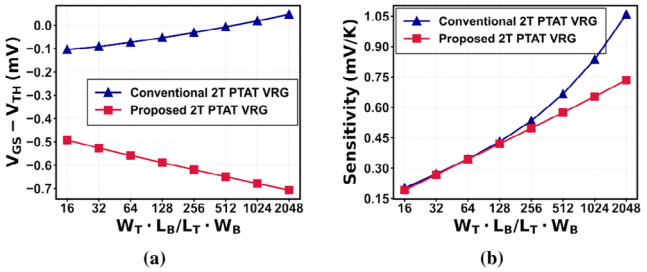


FIGURE 2 | (a) Simulation results of $V_{GS} - V_{TH}$ for both the conventional and proposed 2T PTAT VRGs as a function of size ratio, (b) T-V sensitivity for both the conventional and proposed 2T PTAT VRGs as a function of size ratio.

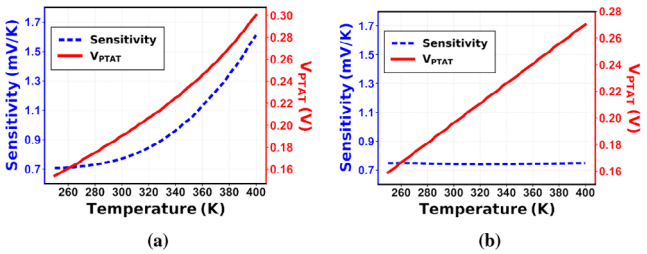


FIGURE 3 | Simulation results of the T–V sensitivity and V_{PTAT} at size ratio of 2048 over the temperature range: (a) conventional 2T PTAT VRG and (b) proposed 2T PTAT VRG.

2T PTAT VRG, the analytical model remains valid at large size ratios because MN_T operates in the deep-subthreshold region [17], allowing for a linear conversion of temperature-to-voltage with high T–V sensitivity. Figure 3 shows the T–V sensitivity and V_{PTAT} at a high size ratio over the temperature range for the conventional and proposed structures.

3 | Proposed 2T CTAT VRG

The proposed subthreshold region NMOS-based 2T PTAT VRG can achieve high T–V sensitivity at high size ratios due to its operation in the deep-subthreshold region. However, the logarithmic increase in sensitivity with the size ratio leads to a significant area overhead for achieving high T–V sensitivity. The simulation results (Figure 2b) indicate that a size ratio greater than 10,000 is required to obtain a T–V sensitivity higher than 1 mV/K. This substantial area consumption restricts the implementation of an on-chip temperature sensors for the ROIC thermal management. Therefore, this letter proposes a PMOS-based 2T CTAT VRG with enhanced sensitivity leveraging the NWE of the 28-nm FD-SOI process.

Figure 1c illustrates the proposed PMOS-based 2T CTAT VRG. In the same manner as the analytical solution of the output voltage of the NMOS-based 2T PTAT VRG, the analytical solution for proposed PMOS-based 2T CTAT VRG is derived by equating the subthreshold currents of MP_T and MP_B. The output voltage

1350911x, 2026, 1, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/el2.70544 by Ewha Womans University Library, Wiley Online Library on [20/05/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

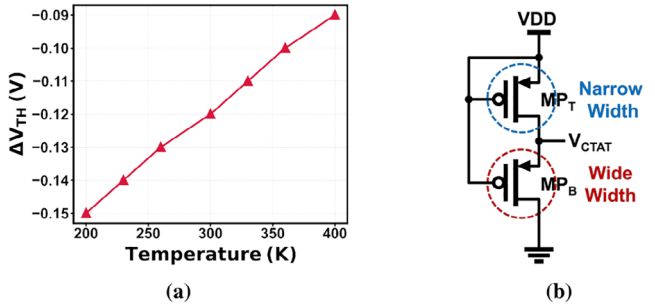


FIGURE 4 | (a) Measurement results of $\Delta V_{TH}(V_{TH}(\text{PMOS}(W = 80\,\text{nm})) - V_{TH}(\text{PMOS}(W = 35\,\mu\text{m})))$. (b) Configuration of wide and narrow width transistors for inducing the NWE in 2T CTAT VRG.

(V_{CTAT}) of the proposed 2T CTAT VRG is derived as follows:

$$V_{CTAT} = \frac{1}{1+\eta_T+\eta_B+\gamma_T} \cdot \left\{ mV_T \cdot \ln \frac{W_T L_B}{L_T W_B} + (1+\eta_T+\gamma_B)V_{DD} - (|V_{TH.T}| - |V_{TH.B}|) \right\}. \quad (2)$$

In previous studies [12–14], the temperature dependence of the threshold voltage difference between stacked-MOSFETs is not considered in the analytical solution. This assumption is valid at small transistor width ratios but becomes inaccurate as the width ratio increases to obtain a high T–V sensitivity. Figure 4a shows the measurement results of the threshold voltage difference (ΔV_{TH}) over the temperature between narrow and wide width PMOSs in the 28-nm FD-SOI process. The threshold voltage is extracted using the constant-current method. In the temperature range above 200 K, the $\Delta V_{TH}(V_{TH}$(narrow width MOSFET) – V_{TH}(wide width MOSFET)) of PMOS shows PTAT behaviour, which is induced from the NWE [18]. From Equation (2), the proposed PMOS-based 2T VRG enhances its T–V sensitivity by employing a narrow width MP_T and a wide width MP_B, utilizing the temperature dependence of ΔV_{TH}.

In this work, the narrow and wide width transistors of the 2T VRG are designed as 80 nm and 10 μ m to induce the NWE [18]. Figure 4b shows the schematic of the 2T CTAT VRG implemented in the 28-nm FD-SOI process, indicating the positions of the narrow and wide width transistors. In addition, stacked-MOSFETs with channel length combinations of 30, 60 and 100 nm are implemented to observe the impact of the DIBL effect on the T–V sensitivity and output voltage. The MOSFET SPICE model has limited accuracy in modelling subthreshold transistor behaviour over a wide temperature range. Therefore, this work experimentally demonstrates a PMOS-based 2T CTAT VRG with enhanced T–V sensitivity from the measurement results.

4 | Measurement Results

Figure 5 shows the measurement setup and layout of 2T VRGs test patterns. To demonstrate the wide-range operation of the proposed 2T VRG, DUTs are measured from 200 to 400 K. Six DUTs are implemented with channel-length combinations of 30, 60 and 100 nm in a 28-nm FD-SOI process. The narrow and wide width transistors of 2T VRGs are fixed at 80 nm and 10 μ m. The

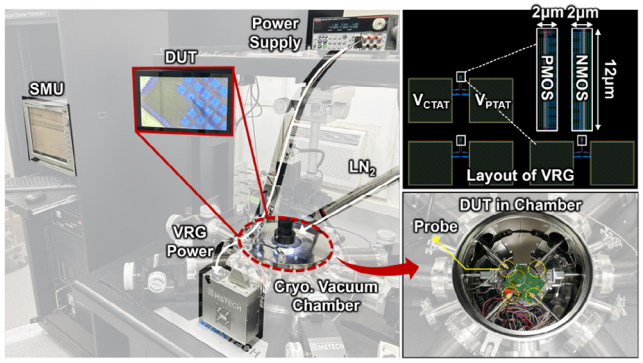


FIGURE 5 | The measurement setup and layout of 2T VRGs test pattern.

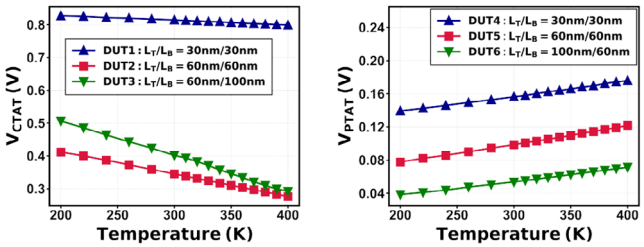


FIGURE 6 | Measurement results of the output voltage over the temperature range of 200 to 400 K: (a) 2T CTAT VRG and (b) 2T PTAT VRG.

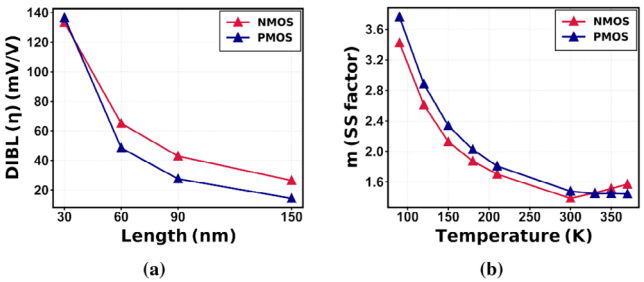


FIGURE 7 | Measurement results of the DIBL and subthreshold slope factor: (a) DIBL as a function of length at 300 K, (b) temperature dependency of subthreshold slope factor of 60 nm MOSFETs.

channel-length information of the implemented 2T VRGs is listed in Table 1.

The measured output voltage of the 2T VRGs is shown in Figure 6 and the T–V sensitivities of the DUTs are listed in Table 1. Except for the DUTs with a 30 nm channel-length, the PMOS-based 2T CTAT VRG shows noticeably higher T–V sensitivity than the NMOS-based 2T PTAT VRG, which aligns with the theoretical analysis. The sensitivity enhancement of PMOS-based 2T CTAT VRG induced by NWE is hardly observed in the 30 nm channel-length MOSFET because of the high DIBL effect. Figure 7a shows the measurement results of DIBL as a function of channel-length.

For the PMOS-based 2T CTAT VRG, the DUT 3 exhibits the highest T–V sensitivity, and for the NMOS-based 2T PTAT

1350911x, 2026, 1, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/el2.70544 by Ewha Womans University Library, Wiley Online Library on [20/05/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

TABLE 1 | Channel-length and T–V sensitivities of fabricated 2T VRGs.

	PMOS-based 2T VRG			NMOS-based 2T VRG		
	DUT 1	**DUT 2**	**DUT 3**	**DUT 4**	**DUT 5**	**DUT 6**
L_{MN_T} (nm)	30	60	60	30	60	100
L_{MN_B} (nm)	30	60	100	30	60	60
$T-V$ sensitivity (mV/K)	0.15	0.69	1.09	0.19	0.23	0.17

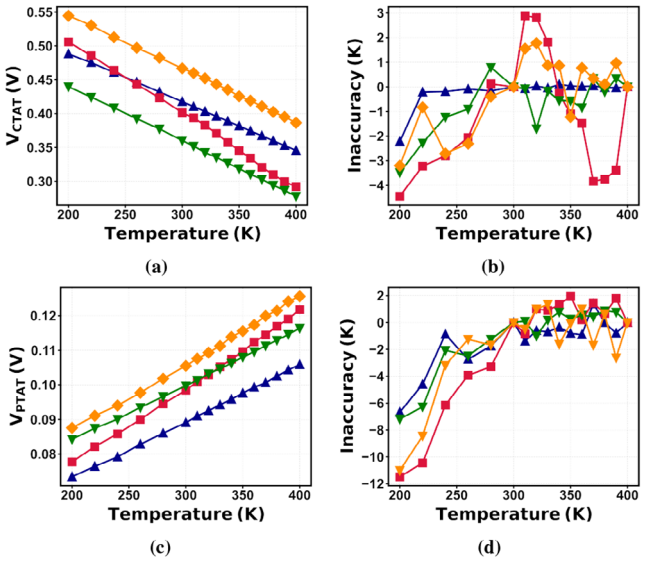


FIGURE 8 | Multi-chip measurement results over the temperature range: (a) output voltages of DUT 3, (b) inaccuracy of DUT 3, (c) output voltages of DUT 5, and (d) inaccuracy of DUT 5.

VRG, the DUT 5 shows the highest sensitivity. This result arises because the T-V sensitivity of the PMOS-based 2T VRG is strongly influenced by the temperature dependence of the threshold voltage difference induced by the NWE. As a result, smaller DIBL of the stacked-MOSFETs leads to higher T–V sensitivity. In contrast, the sensitivity of the NMOS-based 2T VRG is mainly dominated by the size ratio of the stacked-MOSFETs. Therefore, among the 30 and 60 nm channel-length devices, which have the highest size ratios among the DUTs, the 60 nm device with smaller DIBL shows higher T–V sensitivity.

The multi-chip measurement results of DUT 3 and DUT 5 are shown in Figure 8, which exhibit the highest T–V sensitivity among the implemented 2T VRGs. The T–V sensitivity and inaccuracy are extracted after a first-order two-point calibration at 300 and 400 K. The proposed PMOS-based 2T CTAT VRG (DUT 3) shows the minimum and maximum T–V sensitivities of 0.72 and 1.09 mV/K, with a peak-to-peak inaccuracy of −4.44 K/ + 2.88 K, and the proposed NMOS-based 2T PTAT VRG (DUT 5) shows the minimum and maximum T–V sensitivities of 0.16 and 0.23 mV/K with a peak-to-peak inaccuracy of −11.49 K/ + 1.79 K. The increased inaccuracy at low temperatures is attributed to the temperature dependence of the subthreshold slope factor (m). Figure 7b shows the temperature dependence of the subthreshold slope factor (m). Table 2 summarizes the performance of the proposed PMOS-based 2T CTAT VRG and state-of-the-art CMOS-based temperature-to-voltage transducers. The comparison table uses the average T–V sensitivity of the 2T CTAT VRG.

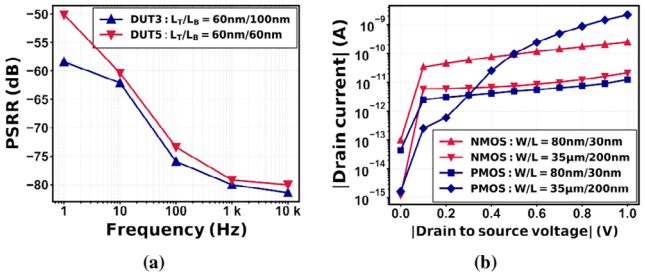


FIGURE 9 | (a) Measurement results of PSRR for DUT 3 and DUT 5 and (b) MOSFETs leakage current at 300 K.

The 2T VRGs are sensitive to supply voltage variation, as shown in Equations (1) and (2). Figure 9a shows the measured power supply rejection ratio (PSRR) of the 2T CTAT VRG (DUT 3) and the 2T PTAT VRG (DUT 5). In the 2T PTAT VRG, the NMOS connected to the supply voltage is designed to have lower impedance than NMOS connected to ground to achieve high T–V sensitivity, making V_{PTAT} sensitive to supply voltage variation. In contrast, in the 2T CTAT VRG, the PMOS connected to the supply voltage has higher impedance, making V_{CTAT} relatively less sensitive.

The power consumption of the 2T VRGs is determined by the MOSFET carrying the larger current among the stacked-MOSFETs. Figure 9b shows the measurement results of the leakage current for the minimum length with a low W/L ratio and 200 nm length with a high W/L ratio MOSFETs. The measurement results indicate that the power consumption of the 2T PTAT VRG is determined by the minimum length MOSFET, whereas in the 2T CTAT VRG, the MOSFET determining the power consumption can shift depending on the temperature, and the increased drain voltage of the wide width PMOS at low temperatures results in relatively higher power consumption than the 2T PTAT VRG.

5 | Conclusion

The proposed 2T VRG follows a subthreshold-current-based analytical model even at high size ratios of the stacked-MOSFETs, enabling high T–V sensitivity. Moreover, the proposed

1350911x, 2026, 1, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/elt2.70544 by Ewha Womans University Library, Wiley Online Library on [20/05/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

TABLE 2 | Performance comparison with state-of-the-art CMOS-based temperature-to-voltage transducers.

	This work	[13]	[12]	[11]
Sensor type	CMOS	CMOS	CMOS	CMOS
Technology	28 nm FD-SOI	28 nm	180 nm	65 nm
Number of Transistors	2	11	14	3
Calibration	2-point	2-point	2-point	1-point
Temperature range (K)	200 to 400	273 to 373	223 to 403	273 to 373
Sensitivity (mV/K)	0.8[a]	0.98[b]	0.49[a]	0.37[a]
Inaccuracy (K)	−4.44/ + 2.88[d]	N.A.	−0.12/ + 3.74[c]	−1.53/ + 1.61[d]
Relative inaccuracy (%)	3.6	2.2	2.61	3.1
Supply (V)	1	0.6	1.2	0.5

[a]Measurement results.
[b]Simulation results.
[c]3-sigma inaccuracy.
[d]Peak-to-peak inaccuracy.

PMOS-based 2T CTAT VRG leverages the NWE to obtain high T–V sensitivity while overcoming the low sensitivity of conventional NMOS-based 2T VRGs. These advantages make the proposed 2T VRG suitable for the large-array temperature-sensor integration for the ROIC thermal management, where low power consumption and compact area are required. Compared with prior works, the proposed 2T VRG exhibits wide operating temperature range and high T–V sensitivity with the fewest transistors. Although the relatively high inaccuracy and low DC voltage level of the 2T PTAT VRGs may limit their applicability to thermal management of ROICs or analogue front-end circuits, the proposed 2T VRGs offer design flexibility, allowing the high size ratio for the system requirements.

Author Contributions

Myung-Hyun Jeon: investigation, conceptualization, writing – review and editing. **Yeonsu Kim:** methodology, software, formal analysis. **Hyunyoung Yoo:** writing – original draft. **Eunji Yoo:** validation, visualization. **Jusung Kim:** writing – review and editing. **Min-Woo Kwon:** writing – review and editing, supervision. **Jae-Won Nam:** project administration, supervision.

Acknowledgements

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), South Korea. This work was supported in part by the National Research Foundation of Korea (NRF) grant, and in part by the IITP-ITRC grant both funded by the Korea Government (MSIT) (RS-2025-24533292, RS-2025-14312970, RS-2025-16063688, and IITP2026-RS-2022-00156295).

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author on reasonable request. The data are not publicly available due to privacy or ethical restrictions.

References

1. B. Sadhu, K. Tien, S. Chakraborty, et al., "Cryogenic CMOS Circuits for Future Scaled Quantum Computing Systems: Challenges and Solutions," in *2025 IEEE Custom Integrated Circuits Conference (CICC)* (IEEE, 2025), 1–3.

2. S. Chakraborty, D. J. Frank, K. Tien, et al., "A Cryo-CMOS Low-Power Semi-Autonomous Transmon Qubit State Controller in 14-nm finFET Technology," *IEEE Journal of Solid-State Circuits* 57, no. 11 (2022): 3258–3273.

3. Y. Zhuo, H. Lu, D. Ma, et al., "A 320× 256 6.9 mW 2.2 mK-NETD 120.4 dB-DR LW-IRFPA With Pixel-Paralleled Light-Driven 20B Current-to-Phase ADC," in *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 68 (IEEE, 2025), 124–126.

4. H. Li, Z. Yang, D. Kong, A. Yin, and P. Zhang, "A 0.037 pJ K^2 338 pW Temperature Sensor Based on Dynamic Leakage-Suppression Logic," *Electronics Letters* 60, no. 16 (2024): 13302.

5. N. G. Toth, Z. Tang, T. Someya, S. Pan, and K. A. Makinwa, "23.7 a BJT-Based Temperature Sensor With ±0.1°C(3σ) Inaccuracy From −55°C to 125°C and a 0.85 pJK^2 Resolution FoM Using Continuous-Time Readout," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)* (IEEE, 2023), 358–360.

6. A. Mosalmani, Y. Rezaeiyan, S. Richter, M. Zamani, Y. Koolivand, and F. Moradi, "A 0.97 nJ/Conversion BJT-Based Temperature Sensor With a Low-Power Two-Stage Dynamic Comparator," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* (IEEE, 2025), 2815–2823.

7. H. Liu, Y. Li, H. Shen, et al., "An Ultra-High Linear Digitization Temperature Sensor Based on SAR ADC With Common-Mode Temperature Drift Suppression," *IEEE Transactions on Circuits and Systems II: Express Briefs* 71, no. 3 (2023): 1047–1051.

8. B. Park, Y. Ji, and J.-Y. Sim, "A 62.6-pJ/Conversion Temperature Sensor With a Capacitor Voltage Division," *Journal of Semiconductor Technology and Science* 21, no. 1 (2021): 73–79.

9. S.-H. Park, J.-H. Boo, J.-G. Lim, et al., "A 232.2 nW segmented curvature compensation sub-BGR with bandgap core reusing," *Journal of Semiconductor Technology and Science* 25, no. 3 (2025): 267–273.

10. M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V," *IEEE Journal of Solid-State Circuits* 47, no. 10 (2012): 2534–2545.

11. H. Wang and P. P. Mercier, "A 763 pW 230 pJ/conversion fully integrated CMOS Temperature-to-Digital Converter With +0.81°C/−0.75°C

1350911x, 2026, 1, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/el2.70544 by Ewha Womans University Library, Wiley Online Library on [20/05/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

Inaccuracy," *IEEE Journal of Solid-State Circuits* 54, no. 8 (2019): 2281–2290.

12. J. Kim, J. Kim, C. Park, M. Yang, and W. Jung, "A Wide Range, Energy-Efficient Temperature Sensor Based on Direct Temperature–Voltage Comparison," *IEEE Solid-State Circuits Letters* 6 (2023): 113–116.

13. J. Tang and X. Tang, "A 12.6-pJ/Conversion Temperature Sensor With 0.98-mV/K Temperature-Voltage Sensitivity," *IEEE Transactions on Circuits and Systems II: Express Briefs* 72, no. 3 (2025): 449–453.

14. S. Jeong, Z. Foo, Y. Lee, J.-Y. Sim, D. Blaauw, and D. Sylvester, "A Fully-Integrated 71 nW CMOS Temperature Sensor for Low Power Wireless Sensor Nodes," *IEEE Journal of Solid-State Circuits* 49, no. 8 (2014): 1682–1693.

15. A. P. Chandrakasan, W. J. Bowhill, and F. Fox, *Design of High-Performance Microprocessor Circuits* (Wiley-IEEE Press, 2000).

16. H. Al-Hertani, D. Al-Khalili, and C. Rozon, "UDSM Subthreshold Leakage Model for NMOS Transistor Stacks," *Microelectronics Journal* 39, no. 12 (2008): 1809–1816.

17. V. Nguyen, F. Schembari, and R. B. Staszewski, "A Deep-Subthreshold Variation-Aware 0.2-V Open-Loop VCO-Based ADC," *IEEE Journal of Solid-State Circuits* 57, no. 6 (2021): 1684–1699.

18. A. Bhardwaj, S. K. Singh, and A. Dixit, "Narrow-Width Effects in 28-nm FD-SOI Transistors Operating at Cryogenic Temperatures," *IEEE Journal of the Electron Devices Society* 11 (2022): 22–29.

1350911x, 2026, 1, Downloaded from https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/el2.70544 by Ewha Womans University Library, Wiley Online Library on [20/05/2026]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License