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IET Circuits, Devices & Systems
Volume 2025, Article ID 4669819, 10 pages
https://doi.org/10.1049/cds2/4669819

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Research Article

Assessment of Data Retainability of 2T DRAM for Processing-In-Memory Application

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Received 24 January 2024; Revised 25 January 2024; Accepted 4 November 2025

Academic Editor: Jin-Xu Xu

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This study examines the influence of cell capacitance on data retention characteristics in dynamic random access memory (DRAM) cells composed of two transistors, in short, 2-transistor (2T) DRAM. The 2T DRAM is gaining attention not only as a standalone memory technology but also as a critical component for processing-in-memory (PIM) applications, offering the full compatibility with standard Si processing. The 2T configuration employs separate transistors for write and read operations, enabling flexible bit-cell design and efficient parallel processing in PIM architectures. However, the small storage node (SN) capacitance, especially when the cell capacitor is truncated, poses challenges for data retention. This work presents a design methodology to enhance data retention in 2T DRAM cells by optimizing transistor dimensions and biasing schemes. Circuit simulations using the 180 nm standard process show that the proposed approach improves retention time by 35% and reduces leakage current by 22% compared to baseline designs. Furthermore, the write transistor current demonstrates a 15% improvement in stability during repeated read operations within the retention time. These results highlight the potential of the proposed design to mitigate retention-related issues and enhance computational accuracy in PIM applications.

Keywords: data retention; dynamic random-access memory (DRAM); processing-in-memory (PIM); Si processing compatibility; two-transistor (2T) DRAM

1. Introduction

In recent years, the exponential growth of data-intensive applications, coupled with the increasing demand for energy efficiency and faster computation, has highlighted the limitations of conventional computing architectures. This has driven a paradigm shift toward device-oriented processing-in-memory (PIM) systems [1–8]. PIM integrates processing capabilities directly within memory modules, reducing data movement and mitigating the bottleneck caused by frequent data transfers between memory and processors. These transfers incur significant latency and energy overhead, restricting the overall performance of traditional computing systems [9, 10]. To address these challenges, PIM cells aim to colocate memory and processing components, enabling computation near data storage. For effective PIM implementation, two critical specifications are required. First, the architecture must support parallel write and read operations to handle large-scale data processing efficiently. Second, it must be compatible with logical processes and adaptable to diverse applications, including those involving central processing units (CPUs), graphics processing units (GPUs), and high-bandwidth memory (HBM) [11–13]. However, existing memory architectures face inherent limitations that hinder their suitability for PIM applications.

Conventional memory technologies such as 6T SRAM and 1T-1C dynamic random access memory (DRAM) exhibit distinct advantages and challenges. SRAM provides high-speed operation and eliminates the need for refresh cycles, retaining data even after read-out [14]. However, its relatively large cell size and conflicting requirements for write and read operations at low voltages make aggressive scaling difficult in

CMOS technology. In contrast, 1T-1C DRAM offers higher bit-cell density and lower static power consumption compared to SRAM, even when refresh operations are considered [15]. These characteristics enable reduced chip size, faster memory access, and higher memory density, making it a highly effective solution for enhancing microprocessor performance within specified power constraints. Despite these advantages, 1T-1C DRAM faces challenges such as complex capacitor fabrication, destructive read operations, and charge-sharing issues during read processes [16]. For PIM operation, in the case of conventional DRAM, a bit-wise operation called triple row activation (TRA) is performed, which performs AND and OR operations using three rows [17]. Also, as it performs destructive read operations, when performing TRA, data previously stored must be copied to another row using RowClone [18] to avoid data loss, and then, TRA is performed to execute AND and OR operations. The 2-transistor (2T) DRAM cell addresses these limitations by utilizing two transistors for independent read and write operations, enabling nondestructive read operations and simplifying the implementation of bit-wise operations such as AND and OR without requiring RowClone. This configuration also offers full compatibility with standard CMOS logic technology, a smaller cell size, and split read/write paths. Furthermore, the 2T DRAM cell demonstrates significant energy efficiency improvements. Its storage capacitance is approximately 20 times smaller than that of 1T-1C DRAM, reducing charging energy by a factor of 20. Additionally, its longer retention time extends the refresh interval from 64 ms in 1T-1C DRAM to 1 s in 2T DRAM, achieving a 15x reduction in refresh frequency [19]. Recent research in 2T DRAM PIM technology has predominantly focused on modifying peripheral circuits. For instance, Zhao et al. [20] introduced switching mechanisms between read and transpose modes within the 2T DRAM array, enabling efficient execution of operations near data storage. While these efforts enhance peripheral design, this study shifts the focus to optimizing the 2T DRAM cell itself. Specifically, it explores the optimization of cell dimensions and biasing schemes to improve data retention.

This paper studies a 2T DRAM cell where the traditional capacitor is replaced with a single transistor. A systematic design methodology is presented, emphasizing transistor dimensions and biasing schemes to enhance retention characteristics. Circuit simulations were conducted using HSPICE, systematically analyzing the impact of various parameters on retention performance. The proposed design demonstrates the potential for overcoming the limitations of existing memory architectures and advancing the application of 2T DRAM in PIM systems.

2. Workflow and Findings in This Work

Increasing the data retention is crucial in DRAM technology. Further, when the capacitor is replaced by a transistor to compose a 2T DRAM cell, the data retention needs to be more carefully managed. Retention time is closely related with the memory bandwidth of a DRAM and gets even more important since a large part of the bandwidth is allocated to times for logic and arithmetic operations with the stored data when the operations are carried out in the memory domain for the PIM applications. Dimensional optimization of the cell and storage transistors making up a 2T DRAM cell has been performed and the effects of negative bias to the cell transistor on data retention have been closely investigated. 2T DRAM structure is highly strategic for realizing the memory domain composed of area-efficient DRAM cell with the conventional full CMOS-only processing architecture in most of the foundry services. It has been succinctly found in this work that the retention time in the second order (s) is achieved from the all-Si 2T DRAM cell by optimizing dimensions and bias schemes, even without a bulky capacitor. Also, the operation of DRAM involves two critical control signals: row address strobe (RAS) and column address strobe (CAS). These signals play an essential role in the read and write operations. RAS selects the row that contains the data to be read or written, while CAS is used to select the column. In the 2T DRAM configuration, these signals enable efficient access to the data stored in the memory cells. Unlike in traditional 6T SRAM, where the entire row is activated during a read or write, the independent read and write paths in a 2T DRAM cell allow more flexible management of RAS and CAS operations. Figure 1 shows the overall workflow in this work for design, characterization, and evaluation of the cell by circuit simulations.

3. Cell Structure and Simulation Strategies

Figure 2a,b shows the schematic of the 2T DRAM cell and the presumed signal flows. Two metal oxide-semiconductor field-effect transistor (MOSFET) transistors are responsible for the write and read operations in Figure 2a, corresponding to the cell transistor and storage transistor in Figure 2b, respectively. Table 1 shows the comparison among SRAM, 1T-1C embedded DRAM (eDRAM), and 2T DRAM that are suitable for the PIM applications, in terms of area and power efficiencies. The read operation is performed independently of the write operation, unlike in either 6T SRAM or 1T-1C DRAM cells. This makes it possible to expect a nondestructive read operation. As a result, the reduction in bandwidth due to data refresh is largely mitigated, which is one of the most advantageous operational features of 2T DRAM cell. Read wordline (RWL) and read bitline (RBL) are used for read access, while write wordline (WWL) and write bitline (WBL) are utilized for write access [21, 22]. This structural and operational configuration enhances flexibility in bit-cell-wise design, as well as read and write margins. Furthermore, mutually independent optimizations of the read and write paths are made possible, making it suitable for parallel processing architecture in PIM applications [20]. On the other hand, it has a drawback in that the capacitance of the node storage needs to be precisely designed with a sufficiently large value to prevent data loss. A shorter RT results in either more frequent refresh operations or lower read current. The former results from the increased frequency of refresh operations, while the latter is due to the rapid lowering of node voltage. Moreover, frequent refresh operations decrease memory bandwidth, or in other words, memory availability, leading to a decline in overall system performance

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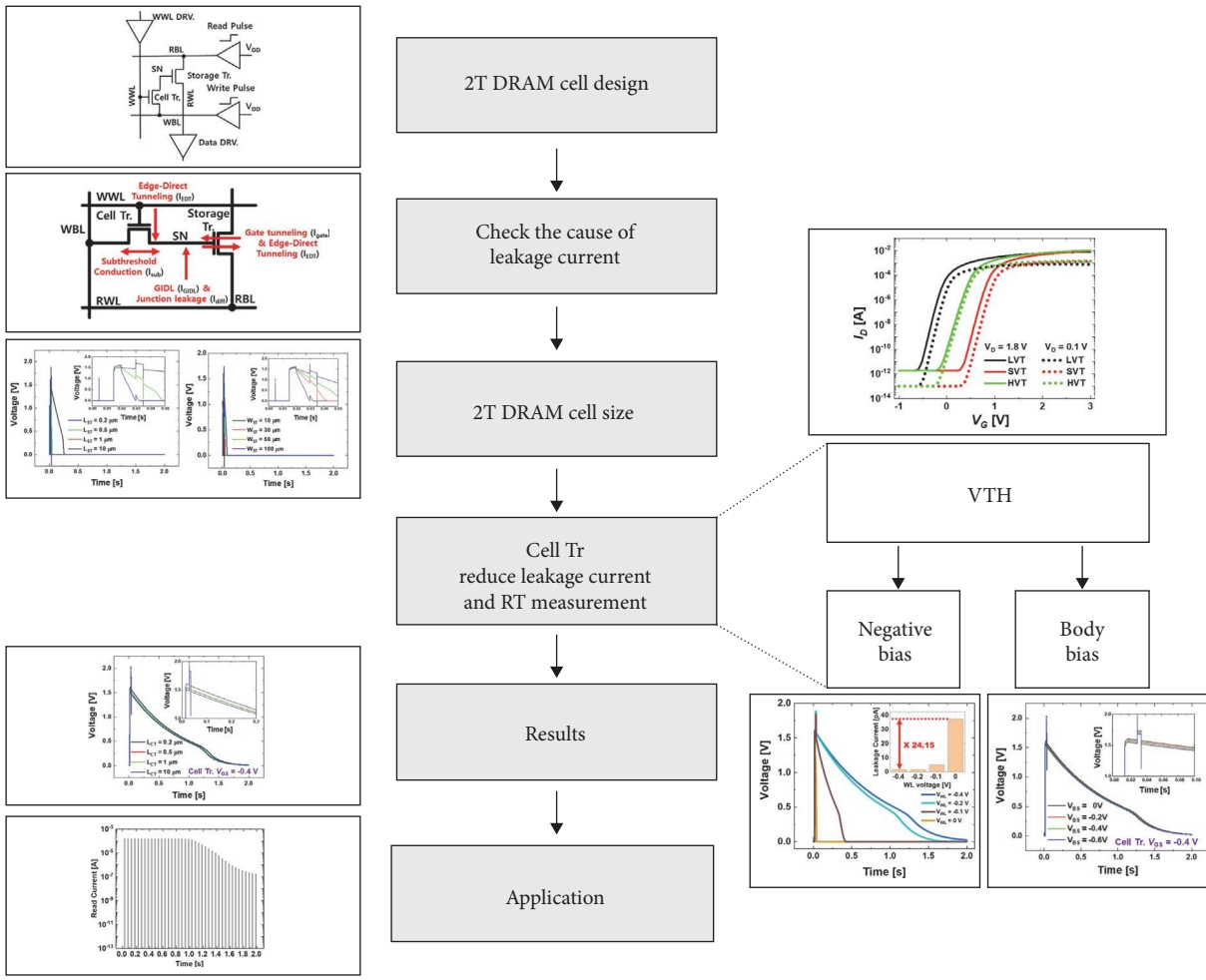


FIGURE 1: Overall workflow in this work for design, characterization, and evaluation of the cell by circuit simulations.

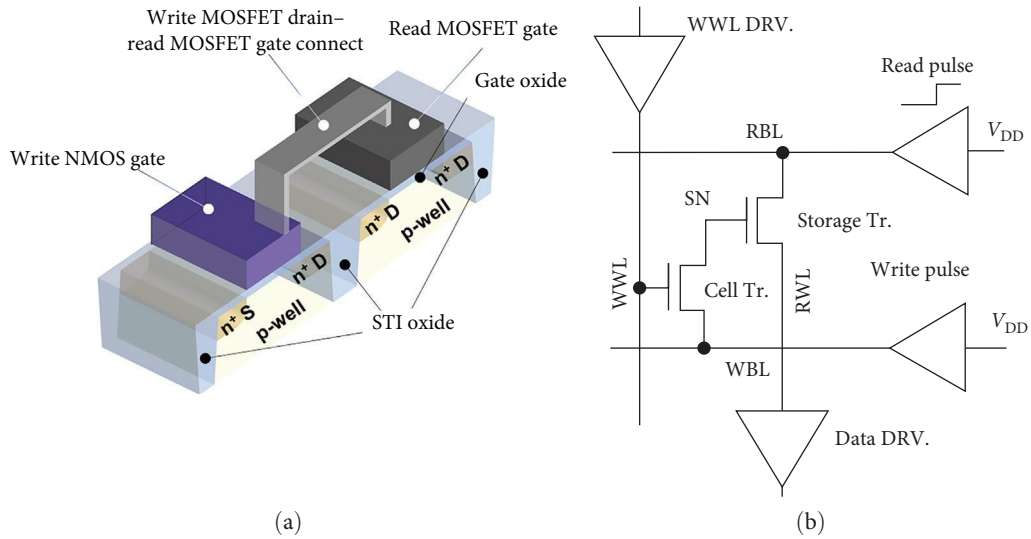
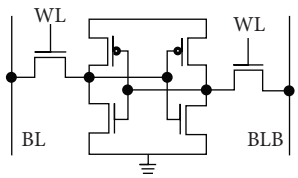
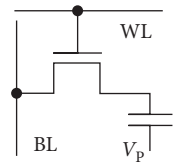
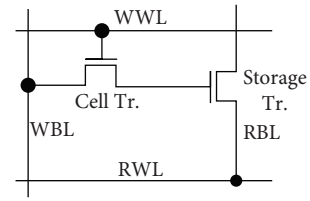


FIGURE 2: Schematic of 2T DRAM cell. (a) Aerial view of a unit 2T DRAM cell. (b) Signal lines for operating a 2T DRAM cell in the array. DRV, driver; RBL, read bitline; RWL, read wordline; SN, storage node; Tr., transistor; WBL, write bitline; WWL, write wordline.

in terms of time and power consumption. Therefore, achieving a practical level of RT and improving random-access speed are still crucial challenges in PIM applications. One of the primary considerations for 2T cell implementation is achieving a longer RT, that is, the time it takes for the level stored on storage node (SN) to deteriorate through leakage currents. Figure 3a shows

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TABLE 1: Comparison characteristic for 6T SRAM, 1T-1C, eDRAM, and 2T cell [19, 21].

Technology features	6T SRAM	1T-1C eDRAM	2T DRAM
Cell schematic			
Process	Logic compatible	+2 (FEOL) +3 (Cap)	Logic compatible
Data storage	Latch (static)	Capacitor (20 fF)	MOS gate (<1 fF)
Static power (ratio)	1x	0.2x	0.19 @500 MHz

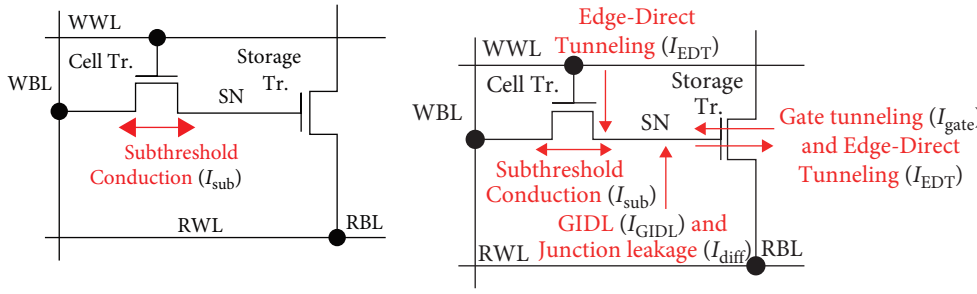


FIGURE 3: Leakage current components in the cell and storage transistors (a) above and (b) under 100-nm CMOS technology [23].

TABLE 2: Comparison between a recent work related with 2T DRAM and this work.

Comparison items	[23]	This work
Solution	– Use of MOSFETs with different V_{TH}'s – Use of PMOS as the cell transistor	– Use of MOSFETs with different V_{TH}'s – Use of negative bias on the cell transistor
Feature	– By using an element with a high V_{TH}, the leakage current is suppressed to prevent the SN from discharge – Low off-state current due to the lower carrier (hole) mobility in PMOS	– Since two n-type MOSFETs make up a 2T DRAM cell in this work, fabrication complexity and area burden are greatly reduced – Suppressing I_{sub} by imposing a negative bias prevents the SN from discharge
Limitations	Area efficiency it substantially lowered due to the *n* well constructed for the PMOS and it takes longer time to write data due to lower carrier mobility in PMOS; in turn, increase in PMOS width is required, which threats the area efficiency increasingly	In addition to V_{DD} and V_{SS}, an additional negative biasing circuit should be implemented

the above-100 nm CMOS nodes. In above-100 nm, subthreshold conduction is the dominant leakage mechanism, compromising data retention in any 2T cell through the channel of cell transistor. Figure 3b shows in CMOS nodes. In below-100 nm CMOS nodes, in addition to subthreshold conduction, including reverse-biased pn-junction leakage (I_{diff}), gate-induced drain leakage (I_{GIDL}), gate tunneling leakage (I_{gate}), edge-direct tunneling current (I_{EDT}), and subthreshold conduction (I_{sub}) have influence [23]. Table 2 shows the comparison between a recent work related with 2T DRAM and this work [23]. The leakage current generated by these components adversely affects the data retention. In this work, for higher accuracy and practicability, process design kit (PDK) for 0.18 µm processing provided by DB HiTek has been utilized in the series of circuit simulations [24].

Figure 4 depicts the signaling time diagram for data verification that can be realized in the 2T DRAM cell-associated circuit in Figure 2b, where WWL and data drivers are added for the complete memory operations of the cell. The drive voltage (V_{DD}) is assumed to be 1.8 V and all the pulse magnitudes in Figure 3 are found to reach V_{DD}. Figure 5a,b shows the transfer and the output characteristics of the cell and

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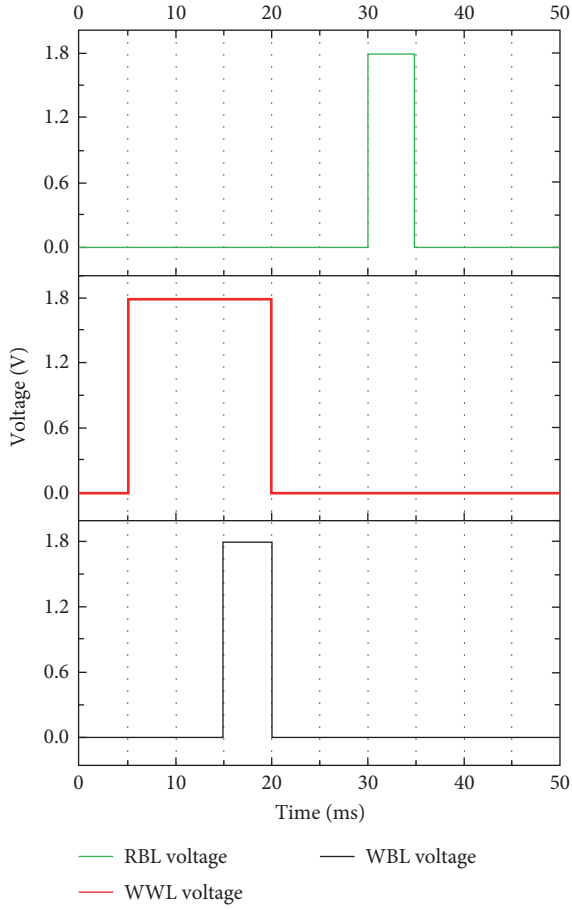


FIGURE 4: Presumably schemed timing diagram of signals for data verification.

storage MOSFETs which are both *n*-type transistors. In order to make fair comparison among the retention characteristics of 2T DRAM cells under different conditions, write signal was applied to the cell transistor through WWL for 5 ms, as can be shown on the bottom row in Figure 4. The change in read current was observed as a function of time after the SN was saturated. It is confirmed by Figure 5a,b that the standard threshold voltage (SVT) NMOSFET is in the subthreshold region at $V_{GS} = 0.5$ V and below. In order to achieve a RT in the order of second, the minimum hold voltage should be $V_{WL} = -0.2$ V as can be confirmed by Figure 5c, by which the decrease in SN voltage by more than 50% compared with the initial value can be stably retarded [25]. Another method is to employ a cell transistor with a high threshold voltage (HVT). Although I_{SUB} is reduced by utilizing a HVT transistor, a higher voltage is required to fully turn it on compared with an SVT transistor (Figure 5a). Figure 5d shows the RTs for the cell transistors with different threshold voltages. A low threshold voltage (LVT) device shows a high leakage current of 10^{-10} A at −0.5 V, about 100 times higher than that of either SVT or HVT transistor, which eventually results in a relatively short RT. On the other hand, for a HVT transistor (WWL = 1.8 V), RT appears to be lower than that of SVT since a HVT transistor is not fully turned on, causing the SN potential to be lower than V_{DD}, as explicitly shown in the inset of Figure 5d. In order to overcome this issue, the WWL voltage needs to be set to $V_{DD} + V_{TH}$ during a write operation, and as a consequence, the SN potential is allowed to reach V_{DD}. This result is similarly witnessed when it comes to an SVT transistor. The reason that SVT (WWL = 1.8 V) and HVT (WWL = 2.2 V) transistors exhibit the similar trends is due to the fact that the leakage currents of the cell transistors are substantially the same as revealed by Figure 5a. The SN is floating in the actual device operations and measurements, so its voltage, the first indicator of data loss, can be only read by simulations. Refresh operation always consumes power for identifying the stored data and recovering it after the destructive read. Also, during a refresh operation, WL is activated sequentially in the row-by-row manner. Thus, while a refresh operation is in progress, other commands cannot be executed within in the same bank. The shorter the RT, the more frequently refresh operations should be performed. Thus, RT is one of the most important performance metrics in DRAM in the sense that it indicates the data integrity closely related with power consumption and bandwidth. As the result, utilizing a HVT transistor in the 2T DRAM cell increases RT so that power efficiency and bandwidth increase are practically achieved. A glitch is observed in Figure 5d, which occurs because the SN that stores data in the 2T DRAM cell is in a floating node state, which leads to capacitive coupling (CC). The operations of the 2T DRAM that influence CC are associated with the application of the WWL pulse during the write operation and the RBL pulse during the read operation. When the first WWL pulse is applied, the SN voltage rises and falls in a manner consistent with the pulse shape due to the gate-drain capacitance (C_{GD}) of the cell transistor. Similarly, when the second RBL pulse is applied, the SN voltage also rises and falls in accordance with the pulse shape, influenced by the C_{GD} of the storage transistor.

4. Results and Discussion

4.1. Maintenance of SN Voltage. In a 2T DRAM cell, the method of storing data involves charging the SN, so maintaining a constant voltage in this region is a crucial aspect of strong data retainability. To keep the SN voltage constant, the size of the storage transistor was controlled since the capacitance due to the gate dielectric of the SN increases with size of the storage transistor. The retention characteristics indicated by SN voltage can be examined while varying the size of storage transistor [26, 27]. Initially, $V_{DD} = 1.8$ V is applied to SN through WBL for performing a write operation, with an enabling signal being applied to WWL. Over a specific amount of time, the SN is charged so that the SN voltage is reached to 1.8 V. Right after the charging is completed, the change in SN voltage is traced with time. During the charge (data) retention, a read operation is continually performed checking if nondestructive operations are achieved. It was observed that the SN voltage increased explicitly during the read operation. This temporary increase was due to read voltage applied to the drain, causing it to be temporarily connected to the SN by gate-to-drain capacitance (C_{GD}), which in turn results in a charge-pumping effect. However, the SN

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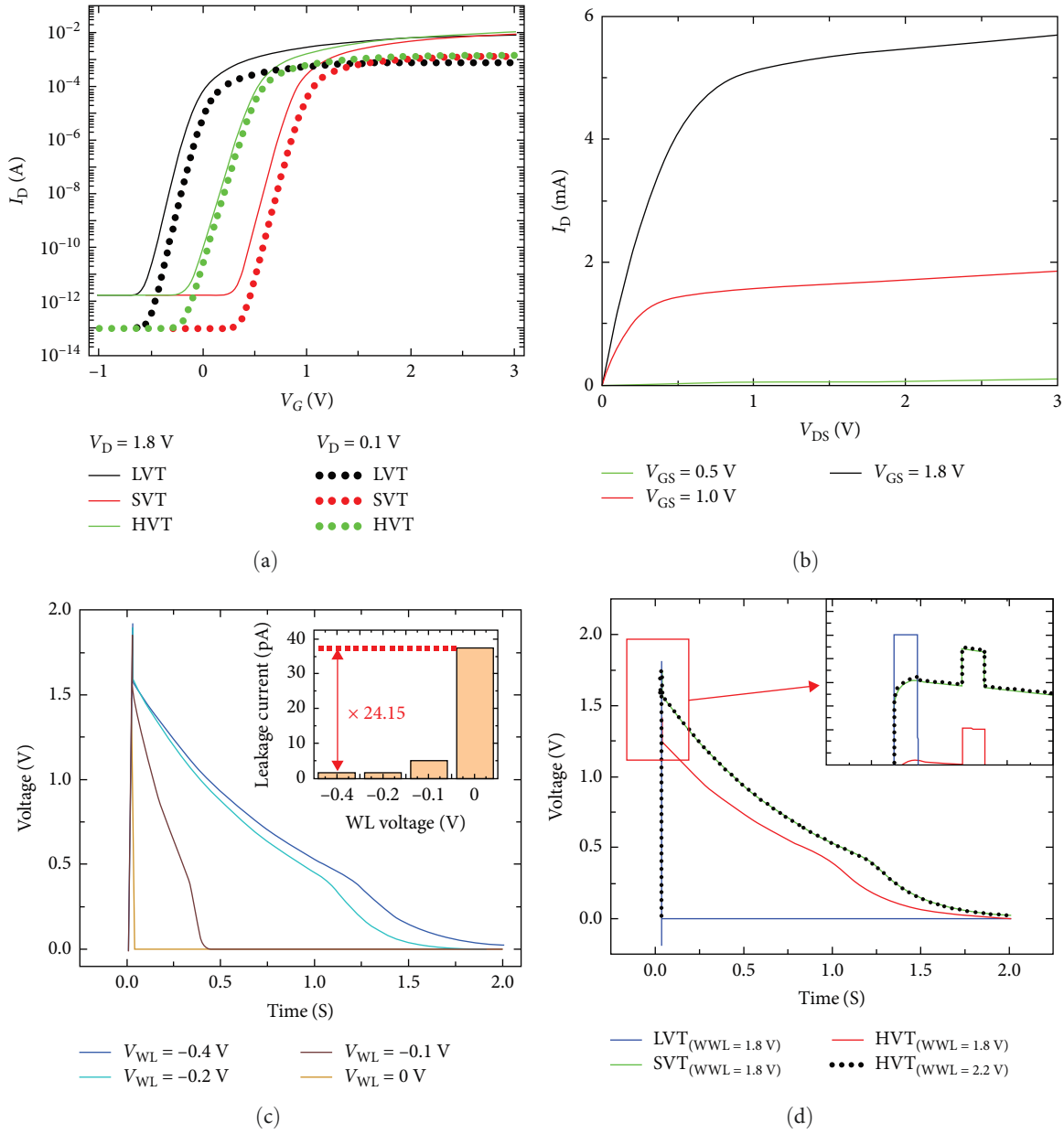


FIGURE 5: Current–voltage characteristics. (a) Transfer and (b) output characteristics of the base transistors. (c) RT for each applied bias when the WL of the cell transistor is inactivated. (d) RT according to the threshold voltage of the cell transistor.

voltage returned its original value after the read operation, having no impact on data retention. Figure 6a shows the investigation of change in SN voltage as a function of time at different channel lengths of the storage transistor (L_{ST}). L_{ST}'s were set to 200 nm, 500 nm, 1 µm, and 10 µm, while the channel width (W_{ST}) was fixed to 10 µm. After applying the voltage to WWL, the voltage on WBL is lowered, and subsequently, it is observed that the SN voltage is elevated up to 1.6 V. The reason that it does not perfectly reach 1.8 V lies in the channel resistance of the cell transistor by which a small voltage drop takes place. As can be confirmed, the discharging from the SN becomes slower as the channel gets longer. However, even with an extension of L_{ST} up to 10 µm, although the RT goes over a known standard of 64 ms, it is substantially limited to 250 ms. Figure 6b depicts the change of SN voltage as a function of time at different W_{ST}'s of the storage transistor. W_{ST}'s were set to 10, 30, 50, and 100 µm, while the L_{ST} was fixed to 200 nm. Being assured by the results, the discharging from the SN gets slower as W_{ST} increase. However, even with an extension of the channel width up to 100 µm, the RT barely exceeded 60 ms. By completely eliminating the capacitor typically found in the 1T-1C DRAM, the charge storage function can be taken over by the capacitor seen from the cell transistor drain to the storage transistor gate. However, it is not so optimistic to obtain a large capacitance from a single transistor, as it is mostly determined by the gate capacitance. Although increasing the length and width of the storage transistor should have

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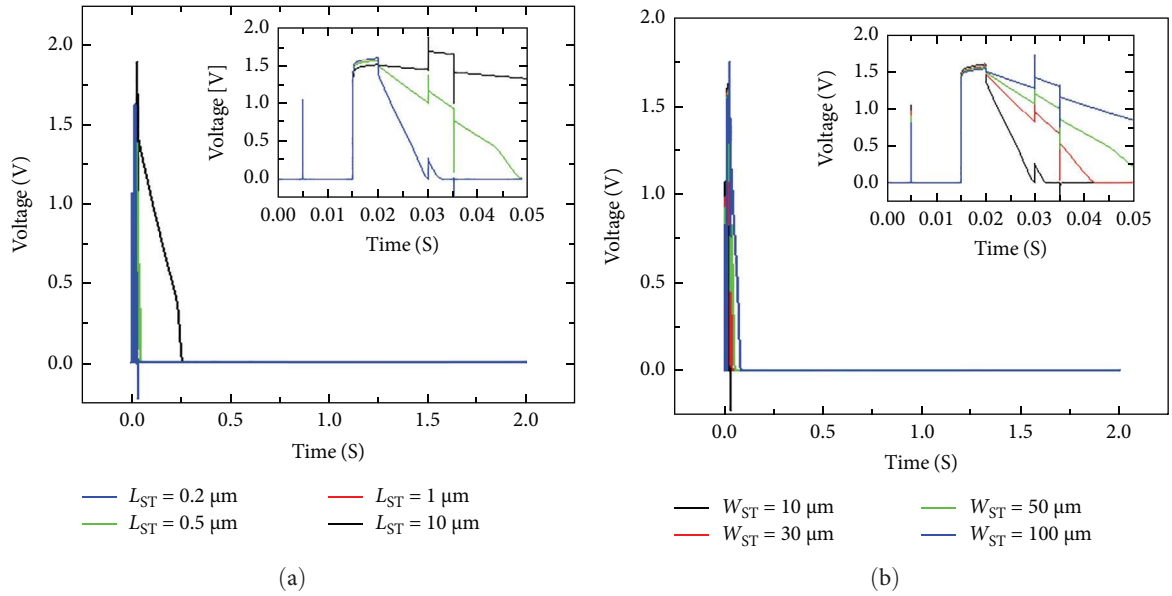


FIGURE 6: Transient changes of SN voltages depending on (a) channel length and (b) channel width of the storage MOSFET.

contributed to an increase in RT, the simulation results reveal that there is a limit to improving the retention solely by controlling the transistor size.

4.2. Suppression of Leakage Current via Cell Transistor. To maintain the voltage of the SN by increasing capacitance, it is possible to enlarge the size of the storage transistor to over 100 μm^2. However, considering the total cell area, it would not be an effective approach. Thus, in order to maintain the SN voltage without a significant sacrifice in area efficiency, other methods need to be exploited. One method to reduce the leakage current through the cell transistor is to lower the gate voltage to turn off the transistor. Examining the I_D–V_{GS} curve in Figure 5a, it is evident that the lowest off-state current is achieved when the V_{GS} drops below −0.2 V. Consequently, the off-state bias on WWL can be reduced to −0.4 V. Figure 5c shows the illustrates the RT for each applied bias when the WL of the cell transistor is inactivated. Thus, Figure 5a,c enable us to observe the extent of influence that the leakage current generated by the subthreshold conduction of the cell transistor has on RT. As explicitly shown in Figure 7a, the RT is notably increased to 1 s. Here, the SN voltage was traced as a function of time for various channel lengths (L_{CT}) of 200 nm, 500 nm, 1 μm, 5 μm, and 10 μm. It is confirmed from Figure 7a that a longer L_{CT} has the effect of increasing the RT. As a result, it can be concluded that suppressing the leakage current of the cell transistor by lowering the off-state gate bias in an efficient way to increase RT. Reducing the standby WWL voltage to negative levels can be a cell-level solution to prolong the time for the charges to be preserved in the SN. However, employing a negative bias in the circuit operation necessitates an additional negative voltage generator and separate power line management scheme, which introduced issues beyond the cell level. To address these problems, the conventional 1T-1C DRAM has opted for a strategy of increasing the threshold voltage (V_{th}) of the cell transistor and raising V_{DD} for DRAM cell operation to 3.0 V or higher [23]. Nevertheless, designing such transistors in a well-defined logic processing integration gives a rise to cost issues and process complexity, which makes it less desirable. Contemplating the methods of negative biasing, another approach can be found with the negative bias to the body. In Figure 7b, the change in SN voltage as a function of time is depicted at different negative biases from 0 V down to −0.6 V with an interval of −0.2 V. Although the negative body biasing also has an effect of increasing the RT, the effect is less significant compare with the scheme of negative gate biasing on the cell transistor. Finally, read operations have been repeatedly performed with the predicted RT and observed the change in read current between read events. After a write operation was carried out, 20 read operations followed continually over 1 s, up to 2 s. Figure 8 demonstrates the envelop of read current of the 2T DRAM cell over time. When taking a closer look into Figure 8, it is evident that a constant read current is plausibly maintained up to 1 s, which is determined by how the charges are strongly secured in the storage transistor. This sustainability of constant read current helps widen the memory bandwidth of 2T DRAM cell, reduce the errors in the computation, and increase the power efficiency in accelerated operation in the PIM applications. All the abbreviations used in the paragraphs are summarized in Nomenclature.

5. Conclusion

In this study, effective methods for enhancing data retention in 2T DRAM cell have been explored. The findings focus on two fundamental approaches: the size of the storage transistor and the characteristics of the cell transistor. While increasing the size of the storage transistor can help maintain the SN voltage to some extent, this effect may be limited when considering the overall chip area efficiency. Instead, the most effective approach to extend the RT of a 2T DRAM cell lies in reducing leakage current through optimal design of the cell transistor. Controlling

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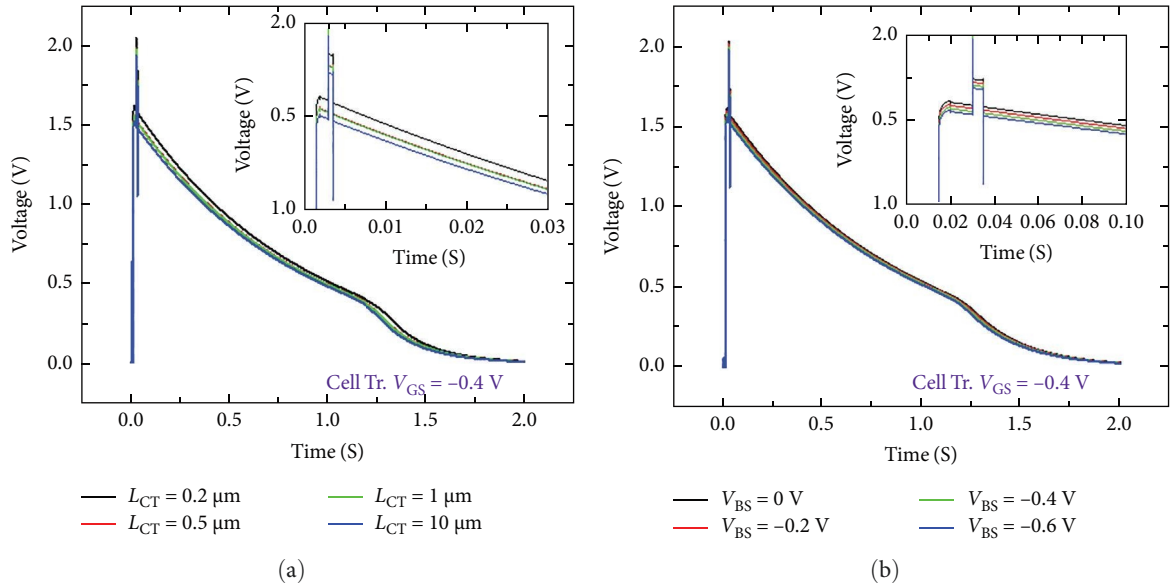


FIGURE 7: Transient changes of SN voltages depending on (a) channel length of the cell transistor and (b) magnitude of negative body biasing.

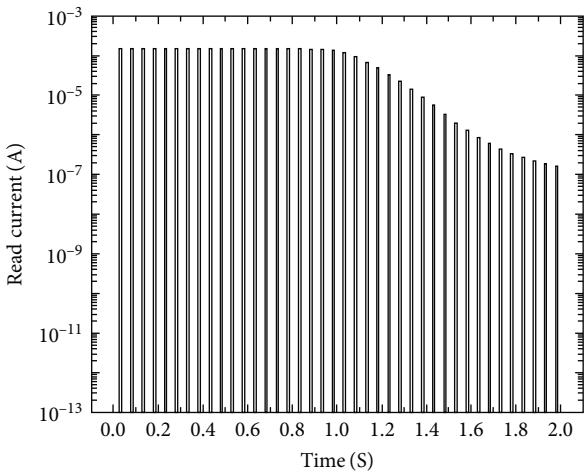


FIGURE 8: Read current of a 2T DRAM cell as a function of time obtained in the more realistic pulsed-mode read operations.

the channel length of the cell transistor may help improve data retainability, but applying a negative bias can have additional impacts. Two locations can be thought as the places where the negative bias can be applied: cell transistor gate and the body of the entire cell. The effect of the former proved to be superior to the latter. The negative biasing has been proven to notably extend the RT into the second-order region. This is substantially beneficial for memory bandwidth, computation accuracy, and operational power efficiency in data-intensive computing within advanced computer architecture, by incorporating the 2T DRAM cell as a logic-and-memory multifunctional component.

Nomenclature

DRAM:	Dynamic random access memory
2T:	2-transistor
PIM:	Processing-in-memory
SN:	Storage node
CPU:	Central processing unit
GPU:	Graphics processing unit
HBM:	High-bandwidth memory
6T:	6-transistor
SRAM:	Static random access memory
1T1C:	One transistor and one capacitore
eDRAM:	Embedded dynamic random access memory
CMOS:	Complementary metal oxide semiconductor
TRA:	Triple-row activation
RT:	Retention time
MOSFET:	Metal oxide semiconductor field-effect transistor
WWL:	Write wordline
WBL:	Write bitline
RWL:	Read wordline
RBL:	Read bitline
I_{diff}:	p–n junction leakage
I_{GIDL}:	Gate-induced drain leakage
I_{gate}:	Gate tunneling leakage
I_{EDT}:	Edge-direct tunneling current
I_{sub}:	Subthreshold conduction
V_{DD}:	Drive voltage
V_{TH}:	Threshold voltage
SVT:	Standard threshold voltage
HVT:	High threshold voltage
LVT:	Low threshold voltage
C_{GD}:	Gate-to-drain capacitance
W_{ST}:	Storage transistor channel width
L_{ST}:	Storage transistor channel length
L_{CT}:	Cell transistor channel length.

Data Availability Statement

All the simulation results and figures were produced by the authors. They need to be cited with proper information on

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Conflicts of Interest

The authors declare no conflicts of interest.

Funding

This work was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT of Korea (MSIT) under Grants 2022M3I7A1078936 and RS-2023-00258527.

Acknowledgments

This work was supported by National R&D Program through the National Research Foundation of Korea (NRF) funded by Ministry of Science and ICT of Korea (MSIT) under Grants 2022M3I7A1078936 and RS-2023-00258527. The EDA tool for circuit simulation was supported by the IC Design Education Center (IDEC).

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