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Article

A Fully Si-Compatible Ni/Si_3N_4/Al_2O_3/p^+ Poly-Si RRAM Device for Analog Synapse and Its System-Level Assessment toward Processing-in-Memory Applications

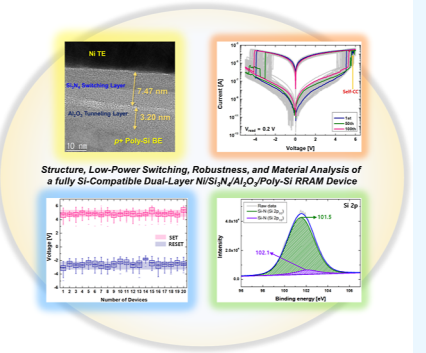
Yeji Lee, Soomin Kim, Seongmin Kim, Wonbo Shim, Sungjun Kim, and Seongjae Cho*

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ABSTRACT: We propose a fully Si-compatible resistive-switching random-access memory (RRAM) device consisting of a Ni/Si_3N_4/Al_2O_3/p^+ poly-Si structure for processing-in-memory (PIM) applications fabricated through a process integration with Si CMOS compatibility. By introduction of an ultrathin Al_2O_3 tunneling layer between the Si_3N_4 switching layer and p^+ poly-Si bottom electrode, the leakage current in the high-resistance state (HRS) is suppressed, resulting in stable bipolar switching characteristics with a high on/off current ratio of approximately 10^4, maintained for more than 10^7 switching operations, as evidenced through durability measurements. The retention characteristics were also maintained without degradation for a considerable time (>10^5 s). When potentiation (6.5 V, 3 μs) and depression (−3.7 V, 3 μs) pulses with the same voltage and time conditions were applied, the device exhibited stable conductance change characteristics with high linearity and symmetry, demonstrating its potential for use as an analog synaptic device through repeatable signal modulation. The average conductance changes were 1.72 and 1.60 μS for potentiation and depression, respectively, confirming balanced weighting characteristics. Furthermore, based on experimentally obtained device characteristics, we implemented a VGG-8 convolutional neural network using the NeuroSim 1.4 framework and achieved high inference accuracy (90.25%), along with low latency and high energy efficiency on the CIFAR-10 data set. Thus, the proposed device holds promise for next-generation nonvolatile memory and analog neural network computing, particularly for energy-efficient processing-in-memory architectures.



INTRODUCTION

With the recent emergence of artificial intelligence (AI) technologies, the demand for high-performance computational processing is rapidly increasing.[1−7] However, the traditional von Neumann architecture suffers from limitations in terms of the physical separation between the processor and memory, which requires continuous data transfer during the computation, resulting in a significant system bottleneck.[8−11] This bottleneck not only consumes more power and slows down the overall system speed. Processing-in-memory (PIM) technology, which can overcome this limitation, has gained attention as a promising solution. PIM integrates processing units directly within the memory, thereby reducing data movement and enabling both low-power operation and high-speed computation.[12−17] Resistive-switching random-access memory (RRAM) is emerging as a next-generation memory device owing to its simple metal−insulator−metal structure, excellent scaling characteristics, and nonvolatility.[18−25] Particularly, RRAM is capable of forming multiple resistive states, which has remarkable potential for application as neuromorphic devices that emulate neural synapses.[26−32] Herein, we propose a Ni/Si_3N_4/Al_2O_3/p^+ poly-Si device: a Si-based RRAM structure with excellent Si processing compatibility. By introducing the dual-layer structure of Si_3N_4 and Al_2O_3 as the switching and tunneling layers, respectively, the device effectively suppresses the current in the off state and contributes to improving the on/off ratio to more than 10^5. The device also demonstrates analog synaptic behaviors, including potentiation and depression, and shows excellent endurance and retention characteristics.

EXPERIMENTAL DETAILS

The fabrication process was carried out entirely in a standard Si CMOS facility to ensure compatibility with foundry processes. The bottom electrode was formed by depositing poly-Si via low-pressure chemical vapor deposition (LPCVD) at 620 °C, followed by ion implantation using a medium-current implanter and activation annealing at 1000 °C. The tunneling Al_2O_3 layer was deposited by atomic layer deposition (ALD) at 350 °C, while the Si_3N_4 switching layer was

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deposited by plasma-enhanced chemical vapor deposition (PECVD), which typically reaches ∼350 °C during the process. All these steps are standard in CMOS manufacturing and fall within the typical back-end-of-the-line (BEOL) thermal budget (≤450 °C). Nickel was chosen as the top electrode metal owing to its established use in self-aligned silicide processes and its BEOL-friendly nature.[33−36] A summary of the integrated process sequence and associated thermal conditions is provided in Table 1.

Table 1. Summary of Device Fabrication Steps

step	tool	temperature [°C]
poly-Si deposition	LPCVD	620
ion implantation	medium current ion implanter	room temperature
annealing	furnace	1000
Al_2O_3 deposition	ALD	350
Si_3N_4 deposition	PECVD	350 (predicted)
Ni deposition	E-beam evaporator	not intentionally controlled

Figure 1a presents a cross-sectional transmission electron microscopy (TEM) image of the fabricated RRAM cell, clearly illustrating the vertically stacked structure composed of Ni/Si_3N_4/Al_2O_3/p^+ poly-Si. The image reveals well-defined and sharp interfaces between individual layers, demonstrating the high uniformity and precision of the deposition processes employed. Figure 1b shows the energy-dispersive X-ray spectroscopy (EDS) results of the above cross-section, which show that the elemental distributions of Ni, N, Al, O, and Si were consistent with the material in each layer, indicating that the chemical composition of each component layer was well maintained. For more information on the full fabrication processes, Figure S1a provides the integrated process architecture with all of the process conditions. Figure S1b,c show the device schematic with the layer configuration and an optical microscopy image of a fabricated array. Furthermore, Figure S2a,b present the results of EDS line scan analysis of the same device cross-section and shows that the wt % distribution of each element was clearly separated at the layer boundaries, thereby demonstrating the accuracy of the laminated structure and reproducibility of the process. To assess system-level applicability for neuromorphic computing, we have carried out system-level simulations through a set of widely accepted frameworks.[37,38]

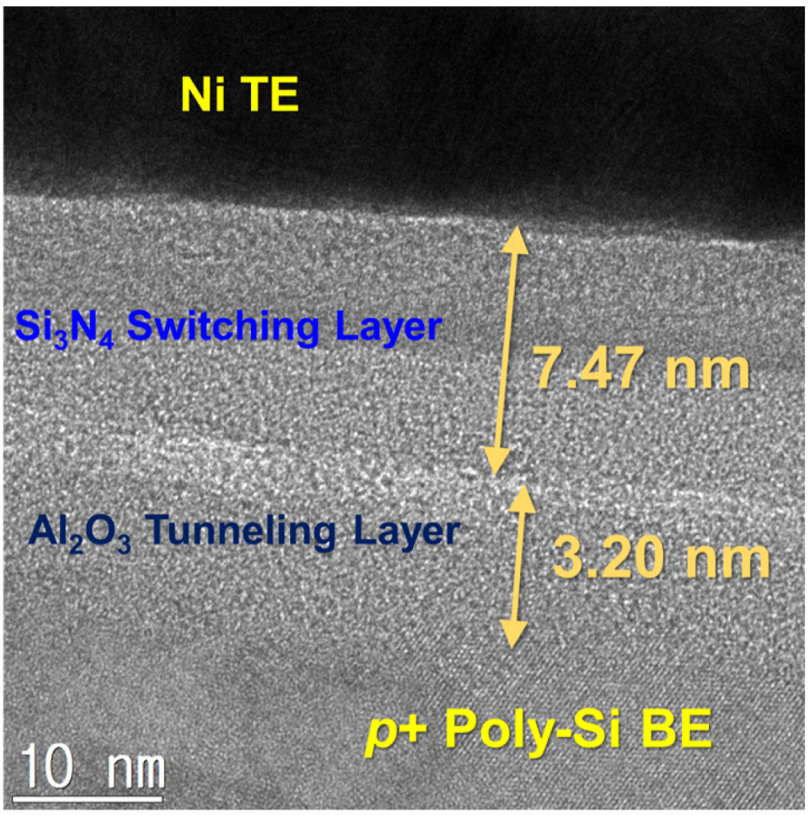
Figure 2a shows the X-ray photoelectron spectroscopy (XPS) spectrum of N 1s, while Figure 2b presents that of Si 2p. The N 1s peak is centered at 397.5 eV, and the Si $2p_{3/2}$ and Si $2p_{1/2}$ peaks appear at 101.5 and 102.1 eV, respectively. These binding energies correspond to Si−N bonding in stoichiometric Si_3N_4.[39−41] The Si_3N_4 film was deposited by PECVD using a gas mixture of 5% SiH_4 diluted in N_2 at a flow rate of 800 sccm, together with NH_3 supplied at 34.5 sccm and additional N_2 at 1000 sccm. The process was performed at a substrate temperature of 350 °C under an RF power of 200 W. These parameters were selected based on reported studies showing that a moderate NH_3/SiH_4 ratio, high N_2 dilution, and elevated substrate temperature promoted the formation of a stoichiometric Si−N network while suppressing hydrogen incorporation in PECVD Si_3N_4.[42,43] Figure 3 shows the changes in atomic contents with etching time demonstrating the distinctions between the Si_3N_4 switching layer, the Al_2O_3 tunneling layer, and the underlaying SiO_2 isolation layer. At the initial etching stage, high Si 2p and N 1s signals indicate the existence of the Si_3N_4 layer.

As surface etching proceeds, Al 2p and 1s contents drastically increase, representing the transition from Si_3N_4 to Al_2O_3. In the deeper region, a continuous elevation of the Si content is attributed to the exposure of the SiO_2 isolation layer. The p^+ poly-Si bottom electrode was prepared by BF_2^+ implantation at 15 keV with a dose of 2×10^{15} cm^{-2} (tilt 7°) followed by activation annealing at 1000 °C. The resulting films exhibited an average sheet resistance of 475.8 ± 14.6 Ω/□ across five wafers, corresponding to a coefficient of variation (CV) of about 3.06%, which indicates high uniformity. Figure 4a shows the thickness uniformity of the 3.20-nm Al_2O_3 tunneling layer deposited by 26 ALD cycles using trimethylaluminum (TMA) as the precursor at 350 °C, showing a uniformity of 3.20 ± 0.07 nm (mean ± 3σ) across a 6-in wafer. The Si_3N_4 switching layer exhibited a thickness of 7.47 ± 0.27 nm (mean ± 3σ), as shown in Figure 4b.

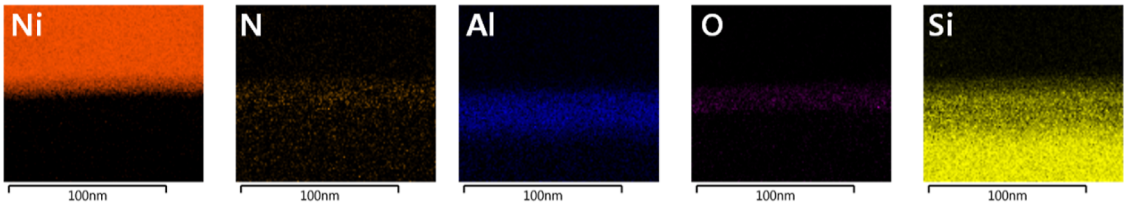
RESULTS AND DISCUSSION

Figure 5a shows the results of DC $I-V$ measurements performed on the fabricated Ni/Si_3N_4/Al_2O_3/p^+ poly-Si RRAM device. The measurements were performed by using a semiconductor parameter analyzer (Keithley 4200A-SCS, Keithley Instruments, Ohio, USA) and 4225-PMU modules in a probe station. Figure 5a also shows that the cycle-to-cycle variation of the resistive-switching characteristics was effectively reduced by carefully adjusting the sweep boundary conditions, such as the starting and ending voltages. Furthermore, the fabricated device operated stably without an external compliance current (I_{CC}), owing to its intrinsic self-compliance behavior, which autonomously regulates the current and suppresses excessive filament growth. Figure 5b demonstrates consistent switching over 100 consecutive DC cycles without failure or distribution broadening. The statistical analysis further reveals that the coefficient of variation (σ/μ) of the set voltage is less than 0.60%, confirming that the optimized self-compliance mechanism effectively minimizes switching variability. These results indicate that stable and uniform switching with a high on/off ratio can be achieved under I_{CC}-free operation, which is highly advantageous for low-power in-memory computing applications. Figure 5c shows a box plot of the extracted set and reset voltages after 100 switching cycles for each of the 20 devices. The switching voltages were stable across all devices with limited device-to-device (D-to-D) variation. Figure 5d shows the cumulative distribution of HRS and LRS resistances measured across the 20 devices. The calculated σ/μ values at a reading voltage of 0.2 V show that the LRS and HRS were 4.28% and 2.33%, respectively. The LRS had a relatively wide distribution owing to the characteristics related to the formation of the filament path as the filaments were formed at random locations in the device each time, resulting in differences in path and thickness. By contrast, the HRS variability was relatively narrow, as the off state was governed by a breakdown or disruption of the conductive filaments, which was more dependent on the uniformity of the insulating layers. Overall, these statistical analyses validate the excellent switching repeatability, and the quantification of both cycle-to-cycle (C-to-C) and D-to-D variability provides a foundation for device-level modeling and system-level design optimization in PIM and neuromorphic computing applications.

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(a)



(b)

Figure 1. Cross-sectional structure and composition analyses of the fabricated Ni/Si_3N_4/Al_2O_3/p^+ poly-Si RRAM cell: (a) cross-sectional transmission electron microscopy image of the vertically stacked dual-layer structure; (b) energy-dispersive X-ray spectroscopy elemental mapping of Ni, N, Al, O, and Si, confirming spatially resolved distribution of each layer component.

Figure 6a shows the endurance characteristics of the fabricated RRAM device, evaluated by applying alternating set (6 V, 500 μs) and reset (−4.5 V, 500 μs) pulses over 10^7 switching cycles. The HRS and LRS states remained clearly distinguishable throughout the entire cycling process, indicating stable and repeatable switching behavior. However, the observed on/off resistance ratio ranged between 10^2 and 10^3, which is relatively smaller than that observed under DC I−V measurements. This discrepancy is primarily attributed to hardware limitations, such as the noise floor and compliance resolution of the pulse-measurement system, which are less sensitive than DC analysis tools. Figure 6b shows the retention performance of the device, measured over 10^5 s using 0.2 V read pulses, applied at l-s intervals. Throughout the measurement time, both HRS and LRS exhibited distinct state retention characteristics, with the LRS maintaining a stable resistance value within a relatively narrow range of variation. To quantitatively validate the distinct resistance state separation, specifically the on/off ratio, additional DC-based endurance data over 500 cycles are presented in Figure S3.

In this work, we demonstrate a fully Si-compatible memristive device that simultaneously achieves self-compliance essential for making up a low-power hardware-driven artificial neural network (ANN), along with the excellent reliability metrics of a large on/off ratio (~10^5), endurance exceeding 10^7 cycles, and data (weight) retention over 10^5 s. As summarized in Table 2, bilayer RRAMs with novel materials, TiO_2/Al_2O_3 or NiO/Nb_2O_{5-x} devices, either required external manipulation for current compliance or showed relatively weak endurance (450 cycles). On the other hand, the Ni/Si_3N_4/Al_2O_3/p^+ poly-Si memristive device in this work achieves self-compliance characteristics without necessitating any external manipulation or limiting component and superb reliability metrics while being fully compatible with the Si CMOS materials and processing tools. All the processes were designed to be conducted under 450 °C, which is highly suitable for the back-end-of-line (BEOL) process to integrate the hardware

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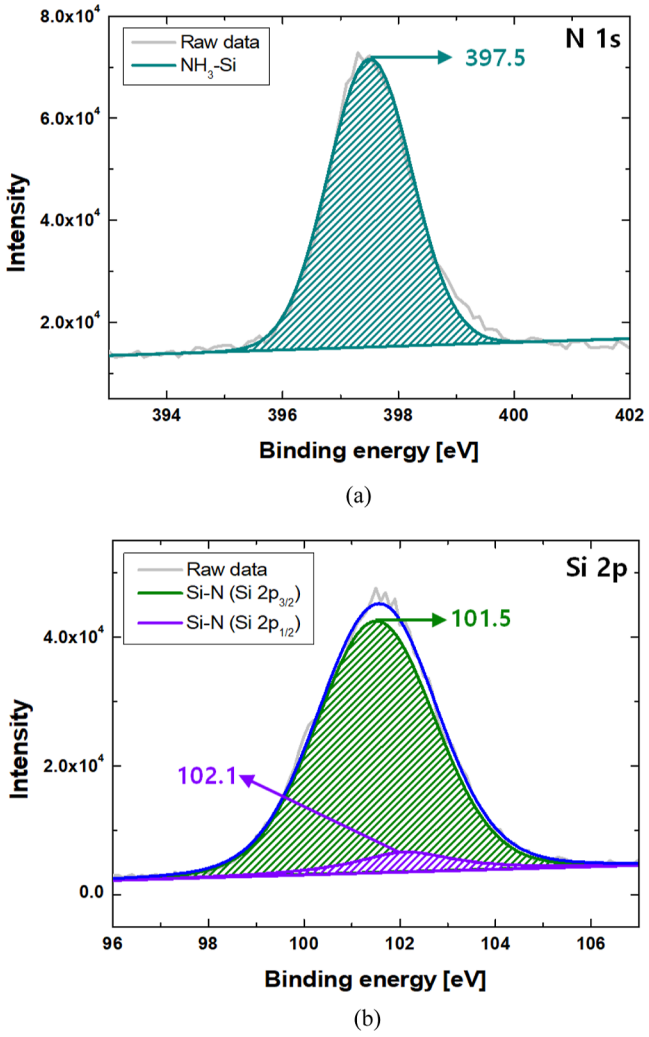


Figure 2. XPS analysis of the PECVD Si_3N_4 film. (a) N 1s peak observed at 397.5 eV. (b) Si 2p peaks at 101.5 and 102.1 eV, corresponding to Si−N bonding.

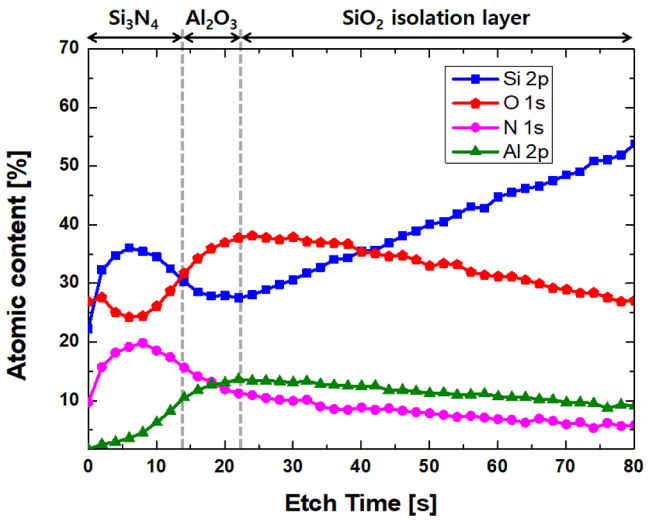


Figure 3. XPS depth-profile of the Si_3N_4/Al_2O_3 stack showing atomic concentrations of Si, N, Al, and O as a function of etch time.

ANN arrays on top of CMOS circuitry without a violation of the CMOS thermal budget.

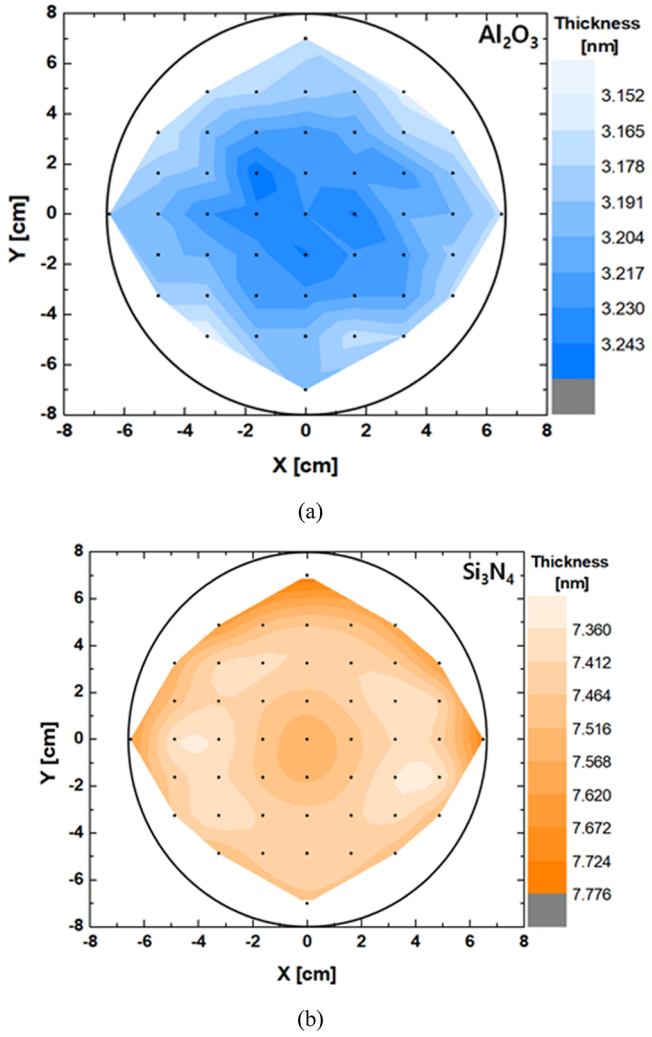


Figure 4. Measurements of thickness and uniformity over the 6-in Si wafers for device fabrication. (a) Al_2O_3 tunneling layer deposited by ALD and (b) Si_3N_4 switching layer deposited by LPCVD.

As shown in Figure 7a, the device without the tunneling layer exhibited ohmic behavior in the HRS with a slope of approximately 1.25 in the low-voltage region, followed by an increase in the slope to approximately 8.92 in the high-voltage region. This rapid increase in slope suggests the possible involvement of a space-charge-limited conduction (SCLC) mechanism, where the traps are filled as the voltage rises and the current increases rapidly thereafter.[47−50] In other words, after the carriers were injected into the traps in the oxide film, the current increased nonlinearly as the traps were saturated. Moreover, for the device with the tunneling layer shown in Figure 7b, the slope started with a relatively low slope (1.58) in the HRS region and increased to slopes of 3.14 and 7.09 in the medium- and high-voltage regions. Particularly, the slope change in the high-voltage region can be interpreted as the involvement of the Fowler−Nordheim (FN) tunneling mechanism.[51−53] FN tunneling is the quantum tunneling of electrons through an insulator barrier as the field increases,[54] which is typically manifested by a sharp increase in current seen in the curve in the high-voltage region. Therefore, the structure including the tunneling layer regulates the field distribution in the oxide film to enable FN tunneling, which contributes to the effective suppression of leakage current in

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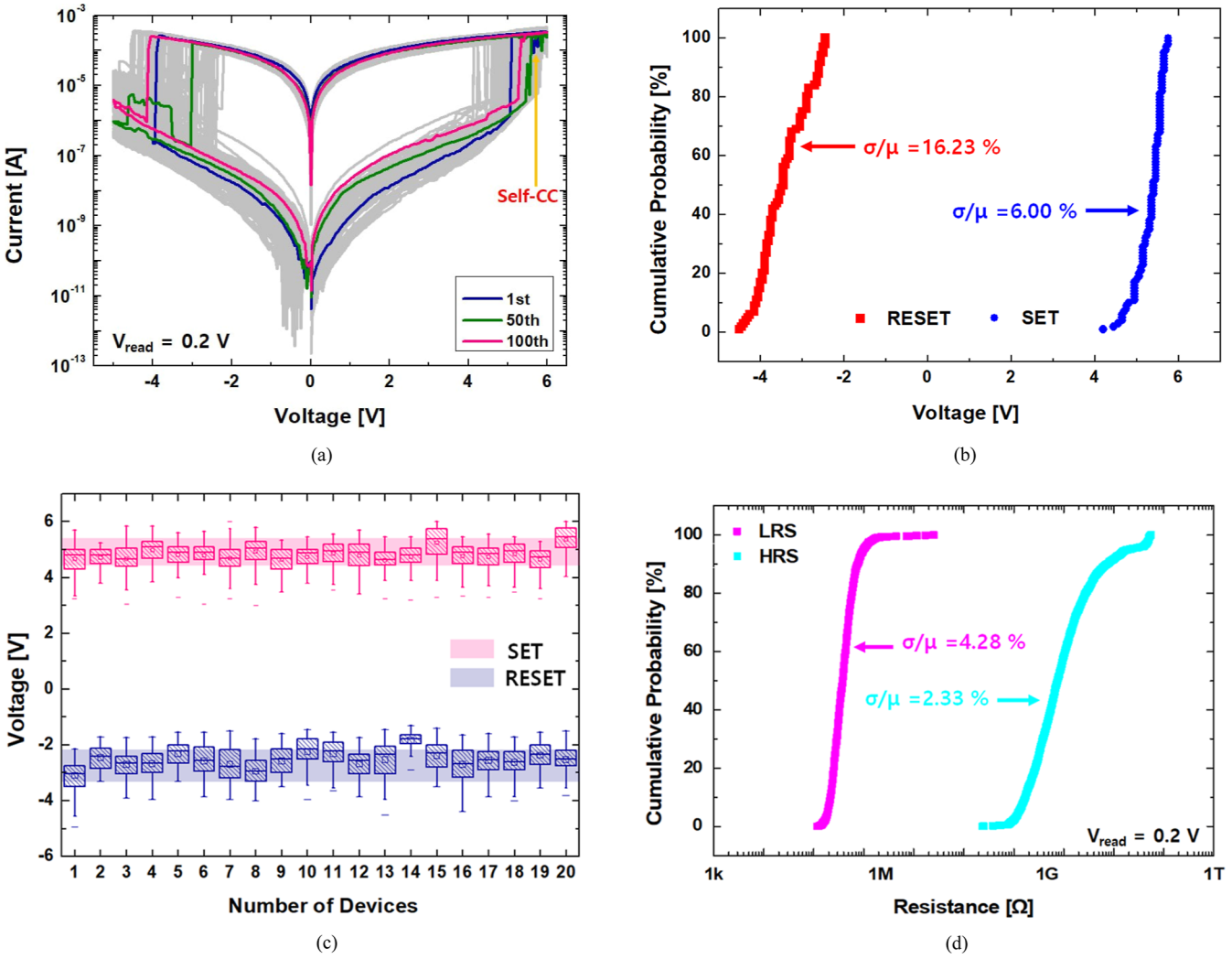


Figure 5. Electrical characteristics of the fabricated Ni/Si_3N_4/Al_2O_3/p^+ poly-Si-based RRAM cell: (a) DC $I-V$ characteristics measured over 100 consecutive cycles on a single device; (b) cumulative probability distribution curve of set and reset voltages measured on a single device; (c) boxplot of set and reset voltages measured over 100 cycles for each of the 20 devices; (d) cumulative probability distributions of LRS and HRS resistances at a read voltage of 0.5 V, based on 100 cycles for 20 devices.

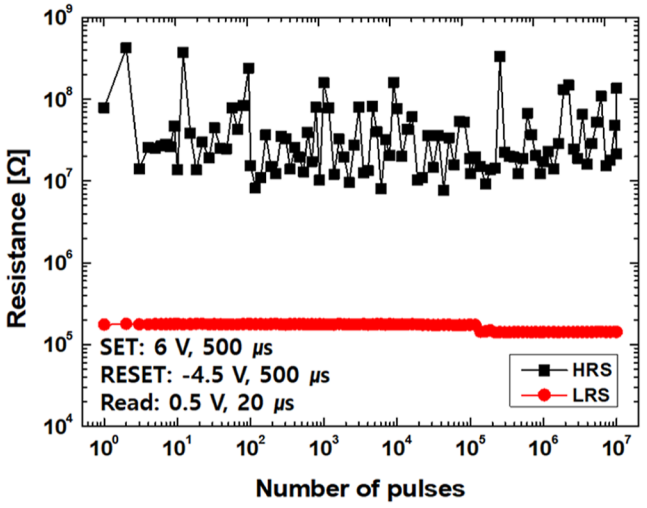
the HRS. The two devices also showed differences in LRS. Devices without a tunneling layer flowed relatively high currents even in the LRS state, which can cause scattering of resistance values and poor stability. By contrast, devices with the tunneling layer exhibited a more stable conduction path with reduced current in the LRS region while still maintaining the ohmic behavior. These results imply that the tunneling layer provides a certain filtering effect on the formation of the current path inside the device, which, in turn, contributes to the improvement of the on/off ratio, switching voltage stability, and energy efficiency of the device. In conclusion, the comparison in Figure 7a,b clearly reveals that the presence or absence of the tunneling layer has a significant impact not only on the conduction mechanisms of the RRAM device but also on its overall electrical characteristics. Specifically, the tunneling layer plays a key role in improving the device performance by inducing and modulating the SCLC and FN tunneling mechanisms through control of traps in the amorphous oxide film and modulation of the field distribution.

Figure 8a shows the long-term synaptic weight modulation behavior of the Ni/Si_3N_4/Al_2O_3/p^+ poly-Si-based RRAM device. Identical pulses were applied for both potentiation and depression—50 potentiation pulses (6.5 V, 3 μs), followed by 50 depression pulses (−3.7 V, 3 μs), repeated for 20 sets, resulting in a total of 2000 pulses. Despite repeatedly applying identical pulses, the conductance change maintained a constant pattern, suggesting a high repeatability and electrical stability of the device. These properties suggest that the synaptic device can reliably control weights in the neuromorphic circuits. The potentiation saturated after approximately 50 pulses, with conductance reaching approximately 90 μS; it was then reduced by depression to a level of approximately 10 μS. The average conductance change (ΔG_{avg}) was calculated using the following equation:[56]

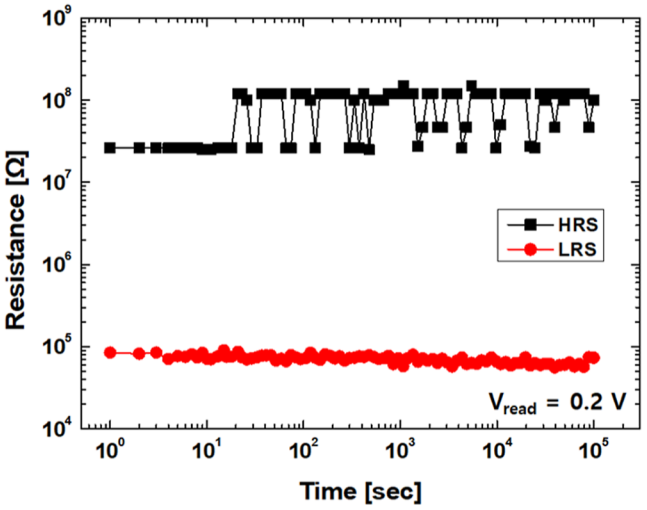
$$\Delta G_{avg} = \frac{G_{max} - G_{min}}{\text{Number of pulses}}$$

The calculated ΔG_{avg} values were 1.72 and 1.60 μS for potentiation and depression, respectively. Therefore, the device had both linearity and symmetry, suggesting that stable analog weighting was possible. To evaluate the technological practicality of the fabricated devices, representative synaptic key performance indicators (KPIs) were extracted, including dynamic range (G_{max}/G_{min}), up/down nonlinearity (α_{up},

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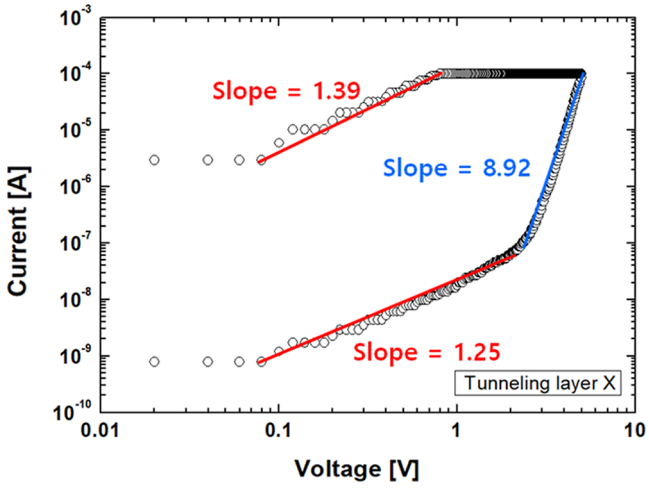


(a)

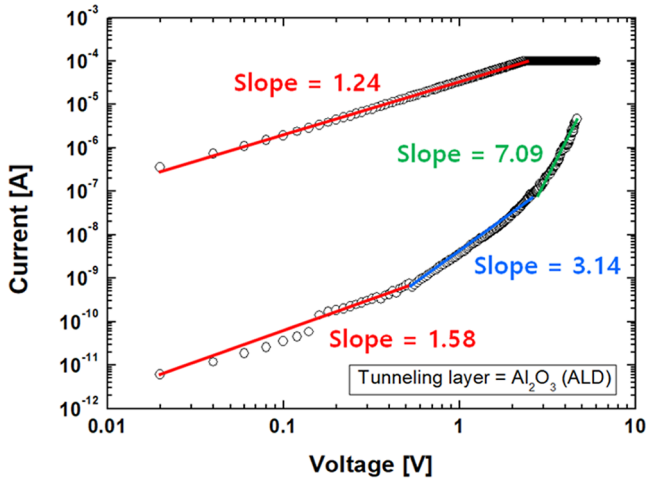


(b)

Figure 6. Pulse-based reliability evaluation of the Ni/Si_3N_4/Al_2O_3/p^+ poly-Si RRAM device: (a) endurance test over 10^7 cycles using set (6 V, 500 μs) and reset (−4.5 V, 500 μs) pulses; (b) retention characteristics measured over 10^5 s using 0.2 V read pulses with 1-s intervals.



(a)



(b)

Figure 7. Log−log scale $I-V$ characteristics of the fabricated resistive-switching random-access memory cell (a) without a tunneling layer and (b) with an Al_2O_3 tunneling layer deposited by ALD.

α_{down}), asymmetry (A), update noise ($\sigma\Delta G$), and effective level count (bits), as summarized in Table 3. In addition, retention measurements of intermediate conductance states were performed, showing stable retention for at least 3×10^4 s, as depicted in Figure 8b. These experimentally obtained KPIs were further incorporated into the system-level simulations, yielding a high inference accuracy of 90.25% on the CIFAR-10 data set. These results demonstrate that the analog characteristics of the proposed device can effectively support high system-level performance, thereby strengthening the correlation between device properties and learning accuracy. Figure 8c illustrates the CNN architecture employed in this study. The network would process input from the CIFAR-10 data set ($32 \times 32 \times 3$), extract features through six convolutional layers (Conv1−Conv6), and pass them through fully connected layers (FCN7 and FCN8) to produce a 10-class classification output. This network was designed to be compatible with RRAM-based neuromorphic hardware and was used to evaluate the practical learning performance of the fabricated synaptic device. Figure 8d shows the classification accuracy of the CNN over 30 training epochs using the measured device characteristics. The accuracy steadily increased and converged above 80%, indicating successful learning using the RRAM-based synapse. Therefore, the high ΔG_{avg}, symmetry, and

Table 2. Comparison of Device Structures and Switching Characteristics

	device structure	compliance	set current	on/off ratio	endurance	cell size
44	TiN/TiO_x/Al_2O_3/IrO_x	required	100 μA	∼11	∼10^6cycles	0.24 μm^2
45	Pt/Ti/TiO_x/TiO_y /Al_2O_3/Pt	not required	<100 μA	∼45	<120 cycles	2.5 × 2.5 μm^2
46	Pt/NiO/Nb_2O_{5-x}/Pt	required	1 mA	10^3 ∼ 10^4	<450 cycles	d = 80 μm
this work	Ni/Si_3N_4/Al_2O_3/p^+ poly-Si	not required	∼300 μA	∼10^5	>10^7 cycles	1 × 1 μm^2

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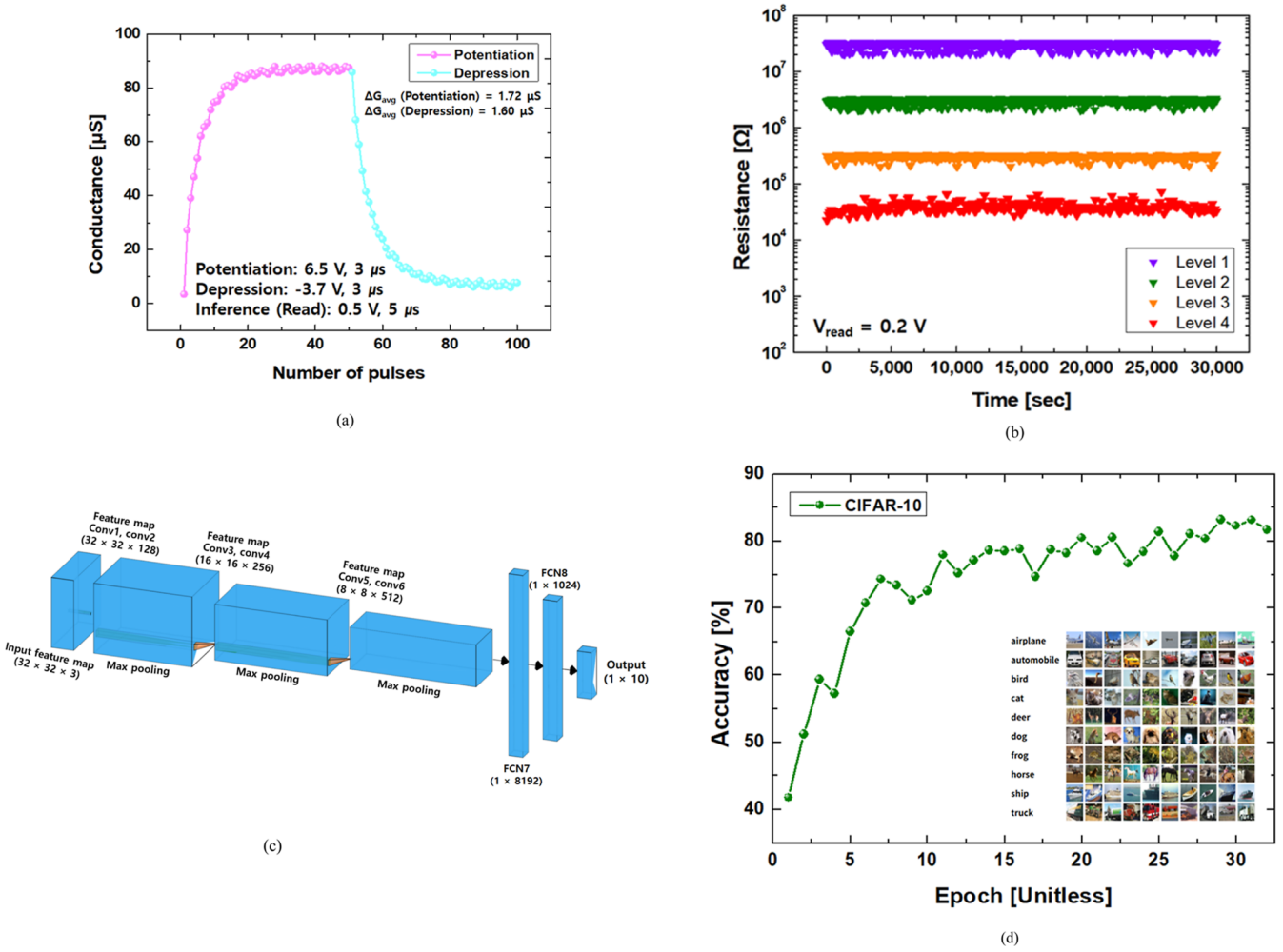


Figure 8. Synaptic characteristics and neuromorphic application of the Ni/Si_3N_4/Al_2O_3/p^+ poly-Si-based RRAM device: (a) linearity and symmetry of conductance modulation under identical potentiation (6.5 V, 3 μs) and depression (3.7 V, 3 μs) pulses; (b) retention of four resistance states at a read voltage of 0.2 V for 3×10^4 s; (c) convolutional neural network architecture used for CIFAR-10 image classification based on the measured device characteristics; (d) classification accuracy trend over training epochs using the fabricated RRAM synapse (inset: exemplary images from the open-source CIFAR-10 data set created by Alex Krizhevsky. Copyright 2025[55]).

Table 3. Standard Synaptic KPIs of the Fabricated Device

dynamic range (G_{max}/G_{min})	14.76
up/down nonlinearity (α_{up}, α_{down})	5.69, 5.31
asymmetry (A)	0.173
update noise ($\sigma\Delta G$, potentiation)	16.87
update noise ($\sigma\Delta G$, depression)	16.98
level count (effective bits)	2 bit (4 levels)

linearity features identified earlier contributed positively to the actual learning performance. Finally, Table 4 summarizes the performance evaluation results at the system's overall system level. Based on CIFAR-10, the following measurements were made: inference accuracy, 90.25%; latency, 4.26 ms; energy efficiency, 2.26 TOPS/W; throughput, 0.30 TOPS; and frames per second (FPS), 240.44. These results quantitatively demonstrate that the proposed RRAM-based device has sufficient potential for practical applications in neuromorphic PIM systems.

Table 4. System-Level Performance Evaluation

evaluations (CIFAR-10)	system-level performance
inference accuracy [%]	90.25
latency [ms]	4.26
energy efficiency [TOPS/W]	2.26
throughput in TOPS	0.30
throughput in FPS	240.44

C-to-C and D-to-D uniformities were systematically evaluated to assess the device reliability. For the C-to-C analysis, potentiation and depression pulses were repeatedly applied for 20 consecutive cycles on a single device. As shown in Figure 9, the conductance update behavior remained highly stable and reproducible, with nearly unchanged conductance states across all cycles.

To further investigate D-to-D uniformity, 10 devices were randomly selected across a wafer, and repeated measurements (10 cycles per device, yielding 100 data sets in total) were performed. The statistical results are summarized in Figure 10a–c. As shown in Figure 10a, the average conductance change was consistently maintained at ~1.7 μS for potentiation and ~1.4 μS for depression pulses. As shown in Figure 10b, the linearity error, expressed as the root-mean-square error (RMSE), remained very small in the range of the 10^{-5}–10^{-4} order. As shown in Figure 10c, the symmetry values averaged ~0.89. The slight deviation from the ideal value of 1.0 is likely

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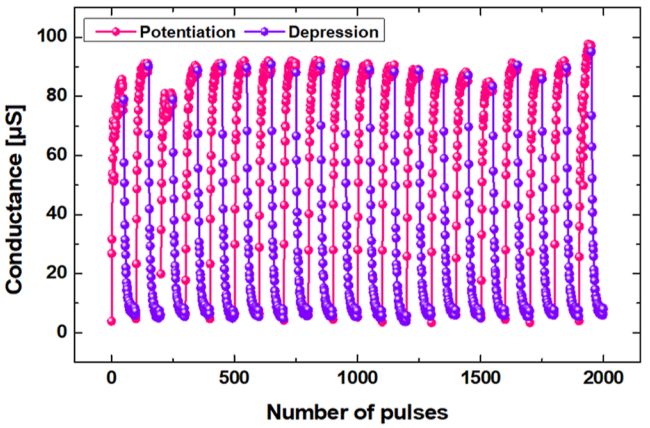


Figure 9. Potentiation and depression behaviors under 20 sets of consecutive identical pulses, where each set consisted of 50 potentiation and 50 depression pulses, making up a total of 2000 pulses.

attributed to the presence of the tunneling oxide. These results confirm reliable uniformities across both cycles and devices, providing quantitative evidence of device robustness.

CONCLUSIONS

In this work, a fully Si-compatible Ni/Si_3N_4/Al_2O_3/p^+ poly-Si-based RRAM device was successfully designed and fabricated. Its resistive switching behavior, electrical reliability, and neuromorphic computing applicability were systematically investigated. DC voltage-based measurements showed that the proposed device reliably exhibited clear bipolar resistive switching characteristics and a high on/off ratio ($\sim 10^5$), which was attributed to the effective suppression of the off-state leakage current by the Al_2O_3 tunneling layer. Pulse-based endurance and retention characterization measurements also confirmed 10^7 repeated switching and long-term data retention over 10^5 s, demonstrating long-term reliability as a memory device. Furthermore, excellent linearity, symmetry, and repeatability were obtained through conductance variation experiments under identical pulse conditions, and these characteristics led to practical application potential through CNN-based neuromorphic learning accuracy and system-level

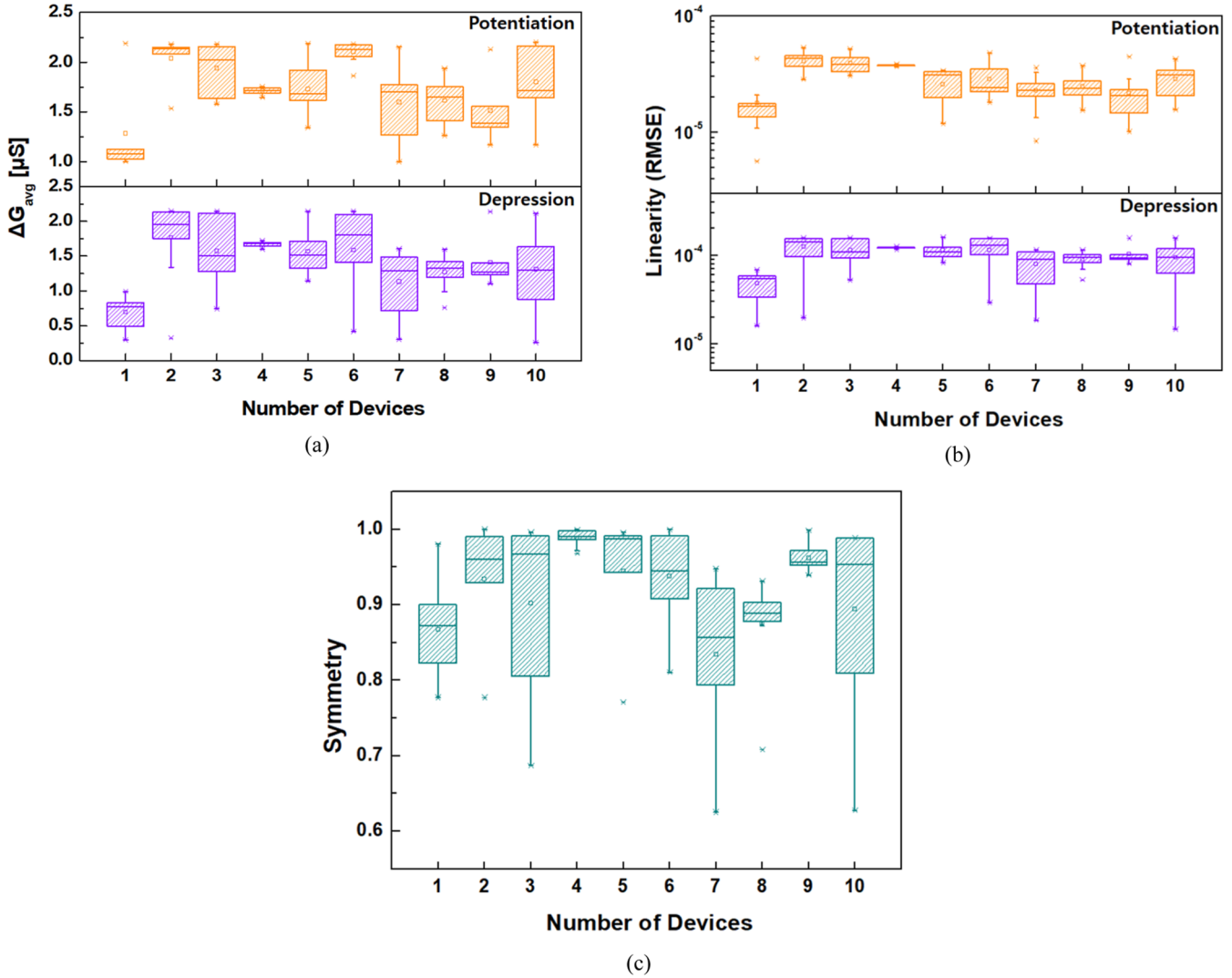


Figure 10. Device-to-device (D-to-D) statistical distribution. Distributions of (a) average conductance change (ΔG_{avg}), (b) linearity of weight modulation in RMSE, and (c) symmetry.

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energy efficiency evaluations. Overall, the proposed RRAM device not only serves as a reliable nonvolatile memory element but also can be a promising candidate for energy-efficient PIM systems, utilizing analog synaptic properties.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.5c08019.

Enlarged optical microscope image of the 10 × 25 crossbar RRAM array, TEM with EDS line-scan analysis results of the Ni/Si_3N_4/Al_2O_3/p^+ poly-Si device, and DC endurance characteristics demonstrating more than 500 switching cycles (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Seongjae Cho − *Department of Semiconductor Engineering, Ewha Womans University, Seoul 03670, South Korea; Department of Electronic and Electrical Engineering, Ewha Womans University, Seoul 03760, South Korea;* orcid.org/0000-0001-8520-718X; Email: felixcho@ewha.ac.kr

Authors

Yeji Lee − *Department of Semiconductor Engineering, Ewha Womans University, Seoul 03670, South Korea*

Soomin Kim − *Department of Electronic and Electrical Engineering, Ewha Womans University, Seoul 03760, South Korea*

Seongmin Kim − *Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, South Korea*

Wonbo Shim − *Department of Electrical and Information Engineering, Seoul National University of Science and Technology, Seoul 01811, South Korea*

Sungjun Kim − *Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, South Korea;* orcid.org/0000-0002-9873-2474

Complete contact information is available at: https://pubs.acs.org/10.1021/acsomega.5c08019

Author Contributions

Yeji Lee refined the process integration, carried out device and array fabrications, measured the fabricated devices, performed system-level simulations, and wrote the manuscript. Soomin Kim performed the layout design and participated in the device and array fabrications. Seongmin Kim participated in the device and array fabrications and set up the pulsed-mode synaptic operation characterization environment. Wonbo Shim evaluated the device characteristics in terms of low-power PIM applications and in part carried out system-level simulations. Sungjun Kim provided the environments for the unit fabrication processes and for the measurement of the fabricated device and array, and evaluated the device characteristics. Seongjae Cho prepared the funding sources, set the research direction, conceived the cell and array structure and process integration, set performance targets, evaluated the fabrication results, device performances, and system-level simulation results, and wrote the manuscript.

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Notes

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■ ABBREVIATIONS

RRAM	resistive-switching random-access memory
HRS	high-resistance state
LRS	low-resistance state
PIM	processing-in-memory.

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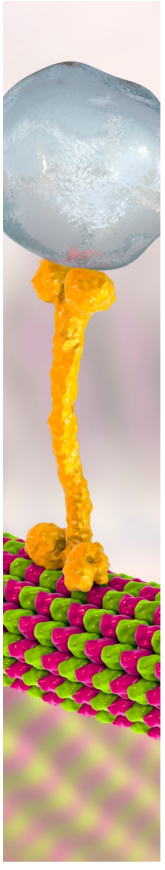
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