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Highly durable and energy-efficient probabilistic bits based on h-BN/SnS_2 interface for integer factorization

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Abstract

As social networks and related data processes have grown exponentially in complexity, the efficient resolution of combinatorial optimization problems has become increasingly crucial. Recent advancements in probabilistic computing approaches have demonstrated significant potential for addressing these problems more efficiently than conventional deterministic computing methods. In this study, we demonstrate a highly durable probabilistic bit (p-bit) device utilizing two-dimensional materials, specifically hexagonal boron nitride (h-BN) and tin disulfide (SnS_2) nanosheets. By leveraging the inherently stochastic nature of electron trapping and detrapping at the h-BN/SnS_2 interface, the device achieves durable probabilistic fluctuations over 10^8 cycles with minimal energy consumption. To mitigate the static power consumption, we integrated an active switch in series with a p-bit device, replacing conventional resistors. Furthermore, employing the pulse width as the control variable for probabilistic switching significantly enhances noise immunity. We demonstrate the practical application of the proposed p-bit device in implementing invertible Boolean logic gates and subsequent integer factorization, highlighting its potential for solving complex combinatorial optimization problems and extending its applicability to real-world scenarios such as cryptographic systems.

KEYWORDS

integer factorization, interface trap, invertible logic gate, probabilistic bit, probabilistic computing

1 | INTRODUCTION

Despite the recent deceleration in the pace of transistor scaling relative to Moore's law projections, advancements in conventional digital computing systems have persisted.[1] These systems have witnessed significant revolutions in machine learning (ML) and artificial intelligence (AI) algorithms. However, without substantial improvements in energy efficiency, the training and operation of large-scale ML models have emerged as major energy concerns.[2] Consequently,

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efforts to extend Moore's law by advancing conventional transistor technology have persisted vigorously. These efforts include three-dimensional (3D) heterogeneous integration,[3] the utilization of lower-dimensional (2D or 1D) materials for channels or interconnects,[4–6] and the exploration of new physical phenomena, such as negative capacitance, tunneling, spintronics, and magnetoelectric effects,[7] to construct more energy-efficient transistors. However, achieving definitive breakthroughs through these approaches remains elusive, as they focus solely on improving transistors for general-purpose computing.

As an alternative approach, there has been a surge of interest in domain-specific computing based on unconventional methods to achieve significant breakthroughs in energy efficiency.[8] Among these approaches, neuromorphic computing stands out as one of the most promising candidates.[9,10] Neuromorphic computing leverages the architecture of biological neural networks, offering functional complexity and adaptability through the massive parallelism of neurons and synapses.[11] A key component for demonstrating neuromorphic computing hardware is the memristor device, which can exhibit highly complex behaviors, particularly biomimetic behaviors, owing to the interacting electro-physico-chemical processes.[12] A single memristor with such complex behavior can functionally replace hundreds or thousands of transistors.[13] Consequently, the interactions among these memristors can lead to higher-level capabilities and significant energy efficiency in computing. Moreover, the architecture of ML can be effectively implemented using crossbar array networks of memristors.[14] This memristor-based network enables the energy-efficient computation of AI-related tasks in various applications, such as image recognition, signal processing, and matrix operations.[15–17]

Nevertheless, concerns regarding the practicality of neuromorphic computing systems remain prevalent due to the variability of memristors. The complex behavior of memristors primarily originates from atomic-scale material changes, which inherently result in a certain level of stochasticity during their operation.[18] These variations, known as cycle-to-cycle or device-to-device variations, fundamentally limit computational accuracy and pose a trade-off between energy and accuracy in computing.[19–21] Because current AI algorithms require high computational accuracy (i.e., they are based on deterministic computation), the intensive application of neuromorphic computing in practical AI tasks remains inevitably restricted.

Notably, recent developments in probabilistic computing (p-computing) offer a completely opposite perspective on the intrinsic variability of memristors.[22] P-computing leverages the inherent stochastic behavior of memristors or other nanodevices as a feature rather than as a limitation, exploiting this stochasticity to perform probabilistic inference. This capability of nondeterministic computation can be used to solve complex combinatorial optimization problems, such as the traveling salesperson problem, integer factorization, Boolean satisfiability, and the knapsack problem, all of which require significant computing resources in conventional digital computing systems.[23] Although quantum computers based on quantum annealing can effectively solve these optimization problems[24] and have already been commercialized (e.g., D-Wave), the requirement of cryogenic temperatures to maintain quantum states poses significant challenges for energy efficiency considerations.[25]

The probabilistic bit (p-bit) serves as a fundamental unit in p-computing hardware, exhibiting probabilistic fluctuations between two binary states over time.[26] External stimulation allows control over the transition probability of each state, effectively rendering it a tunable random number generator. Various p-bits utilizing the inherent stochasticity in different materials and devices have been demonstrated, including magnetic tunnel junctions,[27] diffusive memristors,[28] oscillators,[29] ferroelectric transistors,[30] Si biristors,[31] and floating body MOSFET.[32] The key metrics in the implementation of p-bits currently encompass energy consumption and endurance. The state of a p-bit changes probabilistically according to the input stimulus, and the energy required for probabilistic switching is a critical factor in the energy efficiency of p-computing. As summarized in Table 1, previous p-bits require tens of picojoules of energy for probabilistic switching. Magnetic tunnel junctions consume significantly less energy than others, with switching occurring within a few nanoseconds or less. However, previous studies have not adequately addressed the actual energy consumption associated with p-bits. To perform computational tasks using the output of a p-bit, cooperation with external digital circuitry is necessary[22]; thus, converting the output of the p-bit into digital bits is essential. Therefore, peripheral circuits such as resistors, transistors, and comparators have been co-integrated with p-bits for digitization. Despite this necessity, analysis of the energy consumption of these peripherals has been completely ignored. Specifically, the common method for digitization using a series resistor results in significant static power consumption due to the formation of a short-circuit current path between the power rails. This oversight in accounting for peripheral energy consumption highlights a critical gap in the current understanding of p-bit efficiency.

Another significant concern is the endurance characteristics of the p-bits. Because continuous probabilistic switching over time is fundamental to p-bit operations, the long-term reliability of these state transitions is crucial. However, only a limited number of studies have

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TABLE 1 Comparison of p-bit configurations and performance.

Mechanism	Device structure	Energy consumption per random bitin p-bit device (voltage × current × time)	Peripheral circuits for digitizing	Endurance	Control input and its margin
Low-barrier nanomagnet[27]	Ru/Ta/CoFeB/MgO/CoFeB/Ta/$[Co/Pt]_2$/Co/Ru/$[Co/Pt]_6$/Co/Pt/Ta	2 fJ/bit	Resistor + NMOS Tr + comparator	Not reported	Voltage pulse level 1.4–2.4 V
Volatile threshold switching[28]	$Cu_{0.2}Te_{0.9}/HfO_2$/Pt	5.4 V × 28 nA × 300 μs = 46 pJ/bit	Resistor + comparator	10^6	Voltage pulse level 4.8–5.6 V
Metal–insulator transition[29]	TiN/NbO_x/TiN	128 pJ/bit	Not designed (external processor)	Not reported	Voltage pulse level 1.32–1.46 V
Spontaneous polarization under thermal noise[30]	$Hf_xZr_{1-x}O_2$ transistor	Unclear	Resistor + 2 inverters	Not reported	Voltage pulse level −0.5 to 0.5 V
Single transistor latch[31]	n-p-n bipolar junction	4.4 V × 0.13 μA × 100 μs = 58 pJ/bit	Resistor + comparator	10^5	Voltage pulse level 4.4–4.7 V
Single transistor latch[32]	Floating body MOSFET	110 nW at 3.4 V (= 1.1 fJ/bit)	Resistor + comparator	10^8	Voltage pulse level 3.3–4.0 V
Carrier trapping (this work)	h-BN/SnS_2 transistor	Probabilistic switching = max 3.36 pJ/bit Buffer = max 1.095 nJ/bit	Active switch + buffer	$>10^8$	Voltage pulse width 10 μs to 10 ms

convincingly demonstrated the endurance characteristics, inevitably casting doubt on the robustness of p-bit operations (see Table 1). Furthermore, an unaddressed issue in previous studies is the margin of the input stimulus. In all the previous studies, the output of the p-bits was adjusted according to the level of the voltage pulse. However, as summarized in Table 1, the range of this voltage level (minimum to maximum) is only 0.1 to 1 V. Consequently, even minor noise in the input stimulus can significantly affect the p-bit output. Poor noise immunity is a critical issue that must be resolved to enhance the reliability and practical applicability of p-computing.

In this study, we demonstrate a novel p-bit device utilizing 2D materials, specifically hexagonal boron nitride (h-BN) and tin disulfide (SnS_2) nanosheets. The recent rise in 2D materials, such as graphene and transition-metal dichalcogenides, highlights their potential advantages over 3D materials owing to their inherent absence of surface dangling bonds and minimal defects. In our p-bit implementation, the electron trapping and detrapping processes at the limited number of defects in the h-BN/SnS_2 interface provided highly durable probabilistic fluctuations, enduring up to 10^8 cycles with minimal energy consumption. In addition, static power consumption is mitigated by incorporating a serially connected active switch with a p-bit instead of using a series resistor. This active switch, a transistor based on the same material as the p-bit (i.e., SnS_2), allows for direct integration without additional interconnections, offering higher integrability than previous p-bits. Furthermore, we propose an innovative breakthrough in the margin of input stimulus; the output of our p-bit is determined by voltage pulse width, ranging from 10 μs to 10 ms. This enlarged input stimulus margin provides higher noise immunity, enhancing the robustness of computational results in p-computing.

2 | RESULTS AND DISCUSSION

2.1 | h-BN/SnS_2 transistor and its interface traps

Figure 1A presents a schematic and optical microscope image of as-fabricated p-bit (M1) with a serially connected active switch (M2). Both the p-bit and active switch have an equivalent transistor structure comprising the top gate, source, and drain electrodes on an Al_2O_3/n^+ Si substrate. In these devices, h-BN serves as the gate insulator and SnS_2 as the channel with a shared source electrode. Figure 1B shows high-resolution transmission

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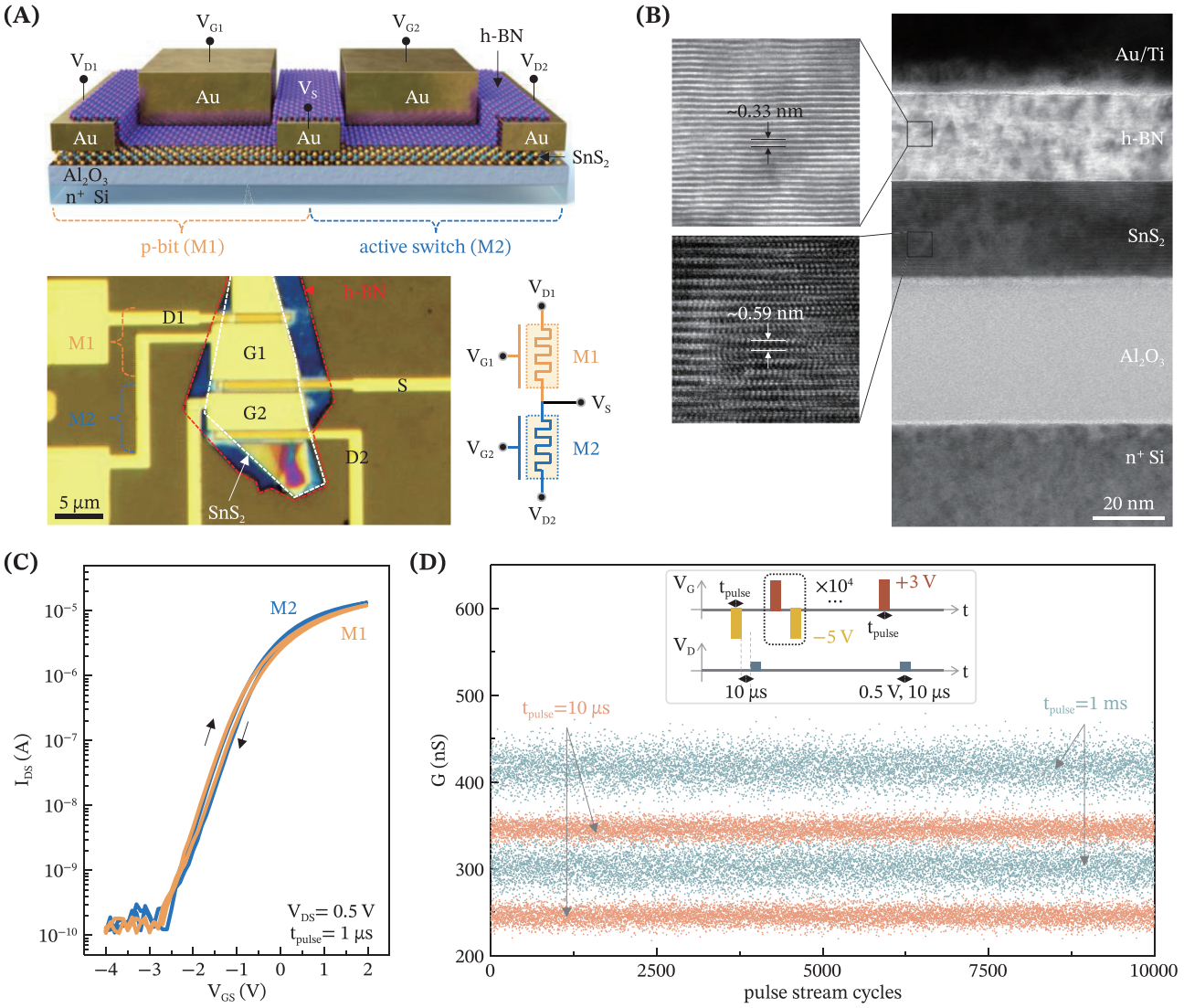


FIGURE 1 h-BN/SnS_2 transistor. (A) Schematics and optical microscope image of the fabricated h-BN/SnS_2 transistor. (B) TEM images clearly reveal the layered lattice structure of both h-BN and SnS_2. (C) Transfer characteristics for both M1 and M2 obtained by the multiple pulsed current–voltage method, with V_G pulse level sweeping from −4 to +2 V under V_D = 0.5 V. The source electrode is always grounded, and pulse width (t_{pulse}) is fixed at 1 μs. (D) The inset shows the one pulse stream cycle to verify the endurance of G modulation. This includes the pulse for G evaluation, before and after the application of 2 × 10^4 pulses for G modulation. Each pulse has an interval time of 10 μs. G modulation was measured during 10 000 cycles of pulse streams, indicating the total pulse application exceeding 2 × 10^8 times. Before each endurance test with different t_{pulse} conditions, the device was initialized through a V_G sweep via the MPIV method, starting from +2 V, decreasing to −4 V, and then returning to +2 V (2 V → −4 V → 2 V), ensuring a stable and reproducible initial state.

electron microscopy (TEM) images of both devices. The h-BN and SnS_2 nanosheets have thicknesses of approximately 23 and 26 nm, respectively. The TEM image reveals a clear layered lattice of both materials; the interlayer spacing of h-BN nanosheets is 0.33 nm,[33] and the spacing corresponding to the (001) interplanar distance of hexagonal SnS_2 is 0.59 nm.[34] Notably, there are no visible polycrystalline areas in the bulk regions of h-BN and SnS_2, suggesting that only a limited number of defects may form at the interface.

To characterize defects at the interface (hereafter referred to as interface traps), the transfer characteristics (drain current–gate voltage: $I_D - V_G$) of both devices were obtained using the multiple pulsed current–voltage (MPIV) method (Figure 1C).[35] This method captures the intrinsic device characteristics while eliminating any effects of the measurement process (see Supporting Information Note 1–1). Notably, when the pulse width (t_{pulse}) was 1 μs and the voltage sweep range was −4 to +2 V, minimal hysteresis was observed in transfer characteristics, indicating

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that these voltage levels and pulse width are insufficient to cause carrier trapping at interface traps. Consequently, accurate extraction of field-effect mobility (μ_{FE}) can be achieved from these trap-free transfer characteristics, yielding a value of 49.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (see Supporting Information Note 1–2). This mobility surpasses those obtained with existing SnS_2 transistors, which commonly exhibit μ_{FE} in the range of 1 to 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$.[36] This improved performance is believed to stem from the MPIV method, which effectively eliminates trap-related degradation during the measurement. Additionally, the use of a top-gate structure may enhance mobility. As studied for other 2D material-based transistors,[37,38] the top-gate configuration allows the gate insulator to act as an encapsulating layer covering the entire channel, reducing the surface roughness and scattering centers commonly found in back-gate configurations.

To further verify the effect of carrier trapping at interface traps on the channel conductance (G), V_G pulses with slightly higher amplitudes (−5 V and + 3 V) than those employed in transfer curve measurements were applied. While larger pulse amplitudes could potentially amplify these effects, they would also increase the risk of device degradation and compromise long-term operational reliability. Therefore, V_G levels of −5 V and +3 V were selected to achieve optimal endurance characteristics under repeated pulse applications. As shown in Figure S5, a positive V_G pulse leads to electron trapping at the interface traps, subsequently decreasing G. Conversely, a negative V_G pulse leads to electron detrapping, thereby increasing G. This modulation behavior of G aligns well with the predictions from the energy band diagram analysis (see Supporting Information Notes 1–3 and 1–4). Notably, this observed G-modulation behavior exhibited remarkable durability. The inset of Figure 1D shows the pulse stream protocol used to assess the endurance of G modulation. To evaluate the long-term reliability and endurance of the device, a pulse stream was applied consisting of alternating V_G pulses (−5 V or +3 V) with a drain voltage (V_D) pulse of 0 V, followed by an evaluation pulse ($V_G = 0$ V, $V_D = 0.5$ V). Each cycle of the pulse stream included 2×10^4 pulses, with G evaluated once per cycle. As shown in Figure 1D, even after 10 000 cycles—corresponding to 2×10^8 pulse applications—the G-modulation behavior remained highly stable, underscoring the outstanding endurance of the h-BN/SnS_2 interface. Furthermore, no significant difference in the endurance characteristics was observed, even when t_{pulse} was increased to 1 ms. It is important to note that the pulse conditions in this experiment were deliberately optimized for endurance testing, rather than for maximizing the contrast between conductance states before and after pulsing.

This high durability is believed to stem from the inherently low density of interface traps at the h-BN/SnS_2 interface. The van der Waals forces between the h-BN and SnS_2 layers facilitated the formation of clean and well-defined interfaces without requiring lattice matching, resulting in a minimal density of interface traps. Previous literature has reported that the inherent interface quality between 2D heterojunctions results in interface trap densities (D_{it}) ranging from 10^8 to 10^9 $cm^{-2} \cdot eV^{-1}$,[39,40] which is several orders of magnitude smaller than that of conventional Si/insulator (such as SiO_2, HfO_2, and Al_2O_3) interfaces. While the high-resolution TEM image (Figure 1B) does not explicitly reveal the defect density at the interface due to the atomic-scale nature of interface traps, the relatively high μ_{FE} observed in our device, compared to other reported h-BN/SnS_2-based transistors, serves as indirect evidence of a low interface trap density. A higher interface trap density would likely result in significant carrier scattering and mobility degradation, neither of which were detected in our measurements. Additionally, the relatively large bandgap of SnS_2 (~2.1 eV) compared to other TMDs likely contributes to a broader energy distribution of interface trap states within the bandgap. This broader distribution reduces the effective density of trap states near the Fermi level. As elaborated in Supporting Information Notes 1–3 and 1–4, not all interface traps contribute to G modulation; their influence depends on their specific energy level positions relative to the Fermi level. The limited extent of G modulation observed in Figure 1D can thus be attributed to the minimal density of interface traps, which ensures consistent robustness even after repeated pulse applications. For a rough estimation in our h-BN/SnS_2 transistor, with gate dimensions of 5.7 μm in length and 8.3 μm in width (as depicted in Figure 1A), and assuming a D_{it} of 10^8 $cm^{-2} \cdot eV^{-1}$ with single-level trap centers, we estimate the presence of only 47 interface traps. While our findings suggest that the interface characteristics of h-BN/SnS_2 play a significant role in the observed device performance, the absence of comprehensive comparative studies across different TMDs under identical experimental conditions remains an issue. Further studies are required to fully validate these observations.

2.2 | Stochasticity in carrier trapping

The stochasticity in carrier trapping is shown in Figure 1D, where the G values obtained by applying V_G pulses exhibit a distribution, indicating cycle-to-cycle variability in the carrier trapping process at the interface traps. To comprehensively investigate this variability, we designed a distinct pulse stream, as shown in Figure 2A (inset). This stream comprises a positive V_G pulse, followed by a negative V_G pulse, which facilitates the continuous trapping and detrapping processes. Owing to

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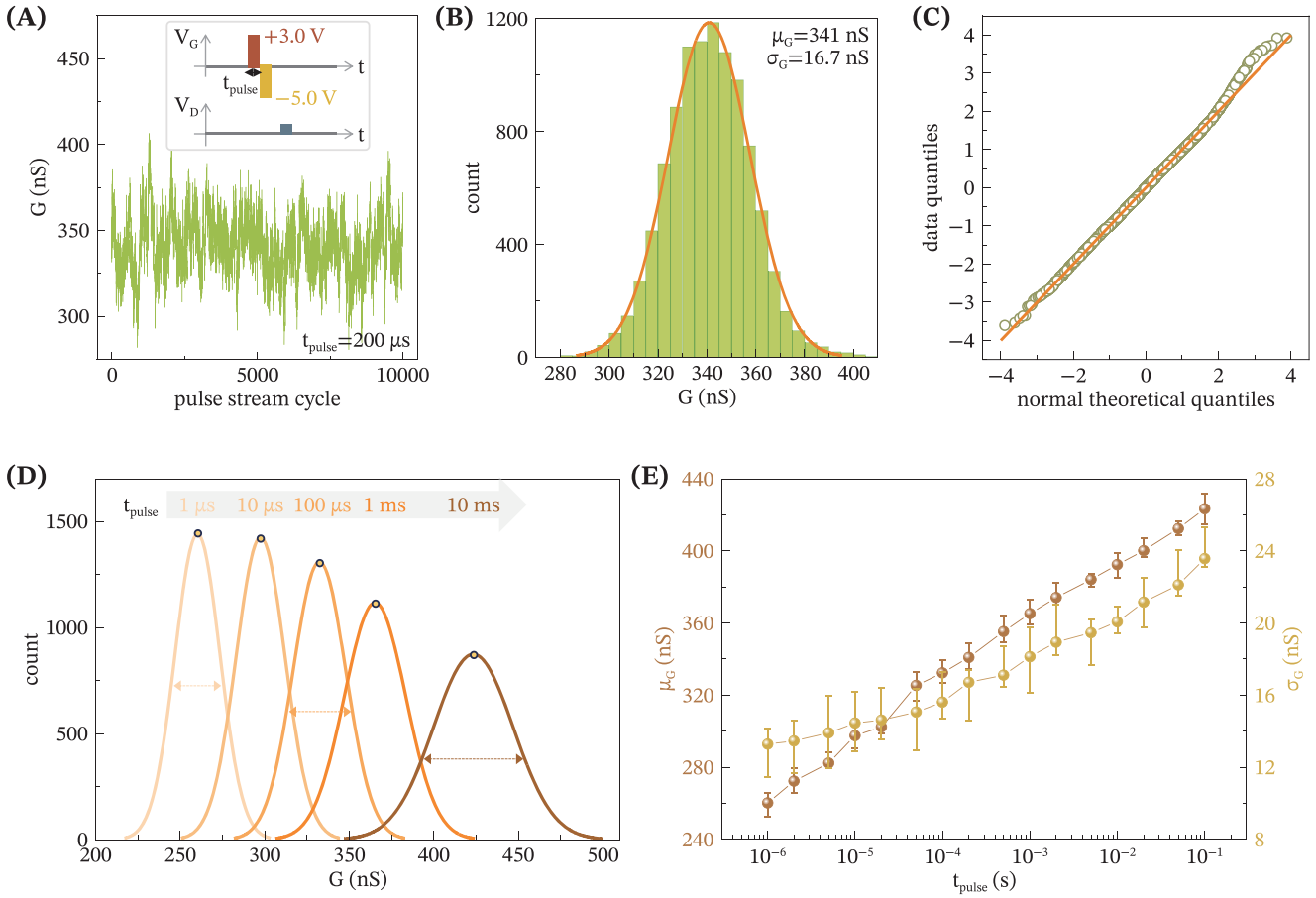


FIGURE 2 Stochasticity of carrier trapping at the h-BN/SnS_2 interface. (A) The inset shows the designed pulse stream to generate cycle-to-cycle variability of the carrier trapping process, where trapping and detrapping processes occur in immediate succession. The data were measured over 10 000 pulse stream applications, with a t_{pulse} of 200 μs. (B) Gaussian-fitted histogram of the data shown in Figure 2A. (C) Q–Q plot further validates the Gaussian distribution. (D) Gaussian-fitted histograms obtained from different t_{pulse}, ranging from 1 μs to 10 ms. To enhance clarity, only the fitted Gaussian distribution curves are depicted (histograms are removed). (E) Summary of μ_G and σ_G according to t_{pulse}. Each error bar represents the maximum, minimum, and median values from a total of 5 evaluation trials (each trial comprising 10 000 cycles of the pulse stream, as shown in Figure 2A).

the intrinsic variability of these processes, G does not precisely return to its initial state. Figure 2A presents the variation in G over 10^4 pulse stream applications, revealing stochastic fluctuations between 280 and 400 nS (a similar behavior was observed in both M1 and M2, as shown in Figure S6). These fluctuations closely approximate a Gaussian profile (Figure 2B), with a mean (μ_G) of 342 nS and a standard deviation (σ_G) of 16.7 nS. This Gaussian characteristic is further corroborated by the quantile–quantile (Q–Q) plot in Figure 2C, where the G quantiles (circles) closely align with the theoretical Gaussian quantiles (line). This random Gaussian distribution results from the stochastic nature of the carrier-trapping process, which is typically observed in charge-trap flash memory devices.[41,42] Notably, the parameters determining this random distribution (i.e., μ_G and σ_G) can be modulated by t_{pulse}. Figure 2D shows the distributions for different t_{pulse}; as t_{pulse} increases, both μ_G and σ_G increase correspondingly (the raw data corresponding to Figure 2D is presented in Figure S7). Repeated evaluation trials exhibited the same trend, as shown in Figure 2E. Each point in the error bar plot represents the maximum, minimum, and median values from five evaluation trials (with each trial comprising 10 000 cycles of the pulse stream, as shown in Figure 2A). While μ_G increases almost linearly with increasing t_{pulse}, some nonlinearity is observed in σ_G. This tunable random distribution can be leveraged to implement a p-bit, as discussed in the following section.

2.3 | p-bit implementation

Figure 3A illustrates the configuration of the as-fabricated p-bit, where two h-BN/SnS_2 transistors are serially connected

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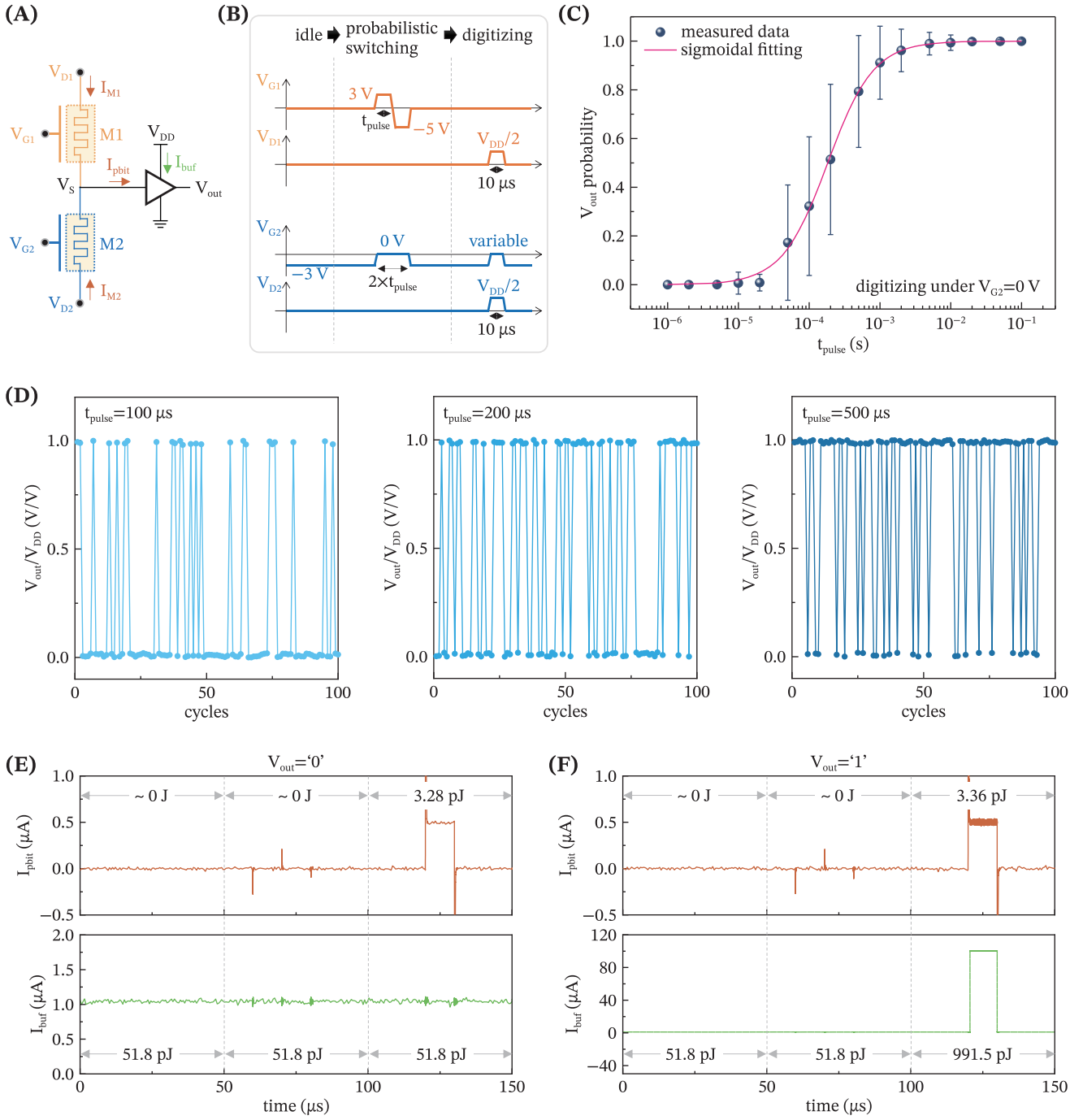


FIGURE 3 p-bit operation. (A) The configuration of our p-bit, including two h-BN/SnS_2 transistors (M1 and M2) with a buffer. (B) The bias conditions for M1 and M2 across one cycle of p-bit operation, delineated into idle, probabilistic switching, and digitizing phases. (C) The V_{out} probabilities under a fixed V_{G2} of 0 V, showing the likelihood of binary outcomes "1" across 30 000 cycles of p-bit operation, with error bars indicating the mean and standard deviation. (D) Representative V_{out} over 100 cycles of p-bit operation for t_{pulse} of 100, 200, and 500 μs, respectively. (E) Measurements of I_{pbit} and I_{buf} during a cycle of p-bit operation with V_{out} at 0 V. (F) Measurements of I_{pbit} and I_{buf} during a cycle of p-bit operation with V_{out} at V_{DD}.

to a shared source electrode (denoted as M1 and M2). M1 generates probabilistic switching, whereas M2 serves as an active switch. The drain currents (I_{M1} and I_{M2}) from these transistors combine at the shared source node, yielding the total source current, $I_{pbit} = I_{M1} + I_{M2}$. This current relationship can be expressed as:

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$$\frac{V_S}{Z_{in}} = G_{M1}(V_{D1} - V_S) + G_{M2}(V_{D2} - V_S), \quad (1)$$

where G_{M1} and G_{M2} denote the channel conductances of M1 and M2, respectively; V_{D1} and V_{D2} are the applied drain biases; V_S represents the potential at the shared source node; and Z_{in} indicates the input impedance of a buffer, assumed to be internally grounded within the buffer. Regarding Equation (1) yields an expression for V_S:

$$V_S = \frac{G_{M1}V_{D1} + G_{M2}V_{D2}}{G_{M1} + G_{M2} + 1/Z_{in}}. \quad (2)$$

According to Equation (2), under the conditions of $V_{D1} = V_{D2} = V_{DD}/2$ and with a high Z_{in}, V_S is maintained very close to $V_{DD}/2$. However, even minor deviations in V_S—resulting from slight imbalances between the channel conductances G_{M1} and G_{M2}—can be effectively amplified by the digitizing buffer. In our design, the buffer acts as a high-gain comparator that converts these small analog variations into a full-scale digital output. Specifically, if G_{M1} is marginally greater than G_{M2}, the small increase in V_S beyond $V_{DD}/2$ is magnified, yielding a digital output of $V_{out} = V_{DD}$. Conversely, if G_{M1} is slightly lower than G_{M2}, V_S falls just below $V_{DD}/2$, and the buffer outputs 0 V. This amplification mechanism ensures that even subtle changes in channel conductance are reliably translated into distinct binary states, enabling robust and energy-efficient probabilistic switching. To minimize the energy consumption, a low V_{DD} of 1 V and a low-power buffer (SN74AUP1G34) were used in our experiments. A detailed experimental setup for the p-bit and active-switch operations is provided in Supporting Information Note 2. Hereafter, for simplicity, the integration of the p-bit and peripheral active switch is referred to as the p-bit.

One cycle of the p-bit operation was divided into three distinct phases: idle, probabilistic switching, and digitizing (Figure 3B). During the idle phase, applying a V_{G2} of −3 V completely turns off M2, preventing a short-circuit current path between the power rails (V_{D1} and V_{D2}). Unlike existing p-bits, which utilize a series resistor, our design employs an active switch, thereby mitigating the static power consumption caused by the leakage current. In the subsequent probabilistic switching phase, M1 undergoes probabilistic switching in response to the applied V_{G1} pulse. Moreover, V_{G2} is set to 0 V to turn M2 on, ensuring that the potentials of both the drain and source nodes for M1 remain at 0 V during probabilistic switching. Importantly, when both V_{D1} and V_{D2} are held at 0 V, the channel current flow and the resulting energy consumption are minimized throughout this phase. In the final digitizing phase, both M1 and M2 are turned on to generate the I_S, with V_{D1} and V_{D2} set to $V_{DD}/2$. Here, M2 plays a crucial role in providing a reference level for the digitization process. Because G_{M2} can be adjusted as desired by varying V_{G2}, the reference level for the digitization process can be easily tuned by adjusting V_{G2} (Figure S9). This capability provides an advantage over existing p-bit implementations that typically employ a comparator with an externally applied reference voltage for digitization.[27,28,31] Existing p-bits require a more complex comparator circuit (compared to our buffer) and additional circuitry to provide the reference voltage, resulting in higher energy consumption compared to the proposed configuration. Consequently, in our p-bit design, the active switch simplifies the circuit configuration and enhances energy efficiency during the p-bit operation (a detailed experimental analysis of the energy consumption is discussed in the next section). Furthermore, because this active switch was fabricated using the same h-BN/SnS_2 transistor, it allowed for higher integrability without the need for additional interconnections.

Figure 3C presents the probability of V_{out} as a function of t_{pulse}. As previously discussed, V_{out} is digitized into either 0 V or V_{DD}, corresponding to binary bit 0 or 1, respectively. Each data point represents the likelihood of observing a binary 1 outcome, derived from 50 cycles of p-bit operations, which collectively define one epoch. This process was repeated across 600 epochs, yielding a total of 30 000 p-bit operation cycles. The mean and standard deviation of these probabilities across the 600 epochs are represented by the data points and error bars shown in Figure 3C. Notably, the V_{out} probability increases with rising t_{pulse}, and the mean values align well with a sigmoidal fitting curve. Figure 3D further illustrates this dependency by displaying representative examples of V_{out} obtained over 100 cycles of p-bit operation. These examples reveal that as t_{pulse} increases from 100 to 500 μs, V_{out} becomes 1 with greater frequency. This trend corresponds to the random distribution of G generated by M1, which shifts to higher μ_G and σ_G values as shown in Figure 2D. Importantly, both the mean and standard deviation values of the V_{out} probability obtained from Figure 3C were incorporated into our p-bit behavior model to accurately capture and represent the stochastic behavior of the device, as detailed in Section 4.3.

2.4 | Unique features of our p-bit

Our p-bit design incorporates several unique features that distinguish it from the existing implementations. As outlined in Table 1, conventional p-bits typically rely on voltage levels as control variables for probabilistic switching, with a narrow input voltage margin of less

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than 1 V. This narrow margin makes the p-computing system highly susceptible to noise. However, this vulnerability has not been sufficiently addressed in previous studies. Our p-bit employs pulse duration (t_{pulse}) to adjust the output probability, spanning an extensive input range from 10 μs to 10 ms. This broader range significantly enhances noise immunity, crucial for developing robust p-computing systems that integrate multiple p-bits. Additionally, concerns regarding high energy consumption for longer pulse durations were effectively mitigated in our design.

To quantitatively assess the energy consumption of our p-bit, we measured the supply current flow (I_{pbit} and I_{buf}) in real time, as shown in Figure 3A. I_{pbit} represents the total current supplied to the drain nodes of the two h-BN/SnS_2 transistors, allowing for an evaluation of their energy consumption. I_{buf} denotes the current supplied to the buffer, which enables a separate assessment of its energy consumption. Figure 3E,F shows the measured I_{pbit} and I_{buf} during one cycle of p-bit operation under the input stimuli shown in Figure 3B. In both instances, t_{pulse} is 10 μs with each phase lasting 50 μs. During the idle and probabilistic switching phases, with V_{D1} and V_{D2} set to 0 V, I_{pbit} exhibited a negligible current, indicating minimal energy consumption by the two h-BN/SnS_2 transistors. Conversely, V_{DD} is continuously supplied to the buffer, resulting in a steady current flow of approximately 1 μA, with the buffer consuming 51.8 pJ during each phase. Here, a notable difference in energy consumption arises during the digitization phase, which is dependent on V_{out}. When V_{D1} and V_{D2} were set to $V_{DD}/2$, I_{pbit} measured approximately 0.5 μA. G_{M1} is slightly higher when V_{out} is 1 than when V_{out} is 0, leading to marginally increased energy consumption of approximately 0.08 pJ. However, the energy consumption of the buffer varies significantly with V_{out}; when V_{out} is 1, it consumes up to 991.5 pJ.

In summary, the energy required for a p-bit operation can be divided into the energy for probabilistic switching and peripheral circuit consumption. The energy consumption of our p-bit h-BN/SnS_2 transistors responsible for probabilistic switching is up to 3.36 pJ/bit, the lowest among existing p-bit implementations, excluding magnetic tunnel junctions (Table 1). In contrast, the buffer consumes a relatively large amount of energy (up to 1095.1 pJ/bit), leading to an overall consumption of approximately 1.1 nJ/bit. The majority is consumed by the peripheral circuit during digitization. Notably, previous p-bit studies have not reported peripheral circuit energy consumption, which complicates direct comparisons. Nevertheless, our design employs an active switch instead of a resistor, and the buffer uses fewer transistors than the comparator, indicating a lower energy consumption in our peripheral circuit than in existing designs. This highlights the fact that the design and optimization of peripheral circuits are crucial for achieving energy-efficient p-computing systems.

2.5 | Invertible Boolean logic gate operation

To validate the feasibility of the p-computing system using our p-bit, we demonstrate invertible Boolean logic gates using Python. The fundamental principles of p-computing have been extensively detailed in the prior literature[22]; thus, we have presented a brief overview herein, with additional details available in Supporting Information Note 3–1. P-computing primarily aims to minimize the energy function of the system (E) governed by the Ising model.

$$E = -\sum_{j \neq i} w_{ij} p_i p_j + \sum_i \theta_i p_i, \tag{3}$$

where w_{ij} denotes the weight representing the connection strength between p-bits, p_i is the output of the ith p-bit, and θ_i represents the external bias. p_i is continuously updated based on the input function (I_i). To achieve energy minimization, I_i is derived by differentiating E with respect to p_i.

$$-\frac{\partial E}{\partial p_i} = I_i = \sum_{j \neq i} w_{ij} p_j - \theta_i. \tag{4}$$

The architecture of a p-bit network for p-computing is shown in Figure S10A, where w_{ij} is determined by the system being addressed. Each p-bit generates a distinct p_i that is fed back to dictate the subsequent input functions, thereby determining the system's minimum energy state. Unlike deterministic computing, which often encounters difficulties in distinguishing incorrect responses arising from the local energy minima, p-computing generates multiple solutions probabilistically, thereby enhancing the capability of achieving the global minimum (Figure S10B). Consequently, p-computing is particularly well-suited for tackling combinatorial optimization problems that are dependent on energy-based models.

Here, we first demonstrate an invertible logic gate function based on a p-bit network. Invertible logic enables the design of a Boolean logic function that can operate in reverse, which is essential for constructing reversible multipliers. These reversible multipliers can then be utilized for integer factorization, which is an example of the combinatorial optimization problem

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discussed in the next section. The implementation of invertible logic gates based on p-bit networks has been reported in previous studies[27,28,31]; further details are provided in the Supporting Information 3–2. We illustrate the implementation of an invertible AND gate as a representative example. A p-bit is assigned to the two input variables (p_1 and p_2) and one output variable (p_y) of the AND gate. The AND relationship between these variables is expressed as $p_y = p_1 \times p_2$. The energy function (E) is then defined as the square of the difference between the target output ($p_1 \times p_2$) and current output (p_y), that is, $E = (p_1 p_2 - p_y)^2$. Subsequently, I_i is derived by differentiating E, as summarized in Table S1. Finally, the physical input stimulus for our p-bit, t_{pulse}, is derived from I_i based on the behavior model of the p-bit (see Section 4.3), where the output probability is well described by the sigmoidal relationship depicted in Figure 3C. Consequently, when t_{pulse}, determined based on I_i, is applied to the p-bits, each p-bit generates a distinct p_i, and these p_i values are again fed back to determine I_i. Through this iterative feedback process, E was minimized.

Figure S11A,B present the results of the forward and reverse AND gate operations, respectively. The forward operation establishes a single output from two inputs, which is analogous to a conventional AND logic operation. In forward operations, p_1 and p_2 are set to 0 or 1, and p_y is determined probabilistically via the p-bit network. For example, Figure S11A indicates that when both p_1 and p_2 are 0, p_y is correctly determined as 0 in approximately 70% of the 500 forward operations conducted, whereas in 30% of cases, p_y is incorrectly identified as 1. Thus, the p-bit-network-based logic gate probabilistically produces incorrect outputs during forward operations. Nonetheless, the true potential of the p-bit network is revealed in reverse operations. In the reverse operation, the p-bit network estimates two input variables that result in a given output. For example, when p_y is fixed at 1, p_1 and p_2 are probabilistically determined, with the likelihood of both p_1 and p_2 being 1 significantly surpassing other combinations (Figure S11B). The unique capability of an invertible logic gate enables the estimation of the likely input variables based solely on the output variable. This capability is further exemplified in other logic operations such as OR and NOT gates, as shown in Figures S12 and S13, respectively.

2.6 | Integer factorization through p-bit network

The combination of invertible logic gates discussed in the previous section facilitates the implementation of more complex logic functions. In this study, we demonstrate an integer factorization function using a p-bit network that represents the reverse operation of a multiplier. Figure 4A illustrates a 2-bit by 2-bit binary multiplication (N = AB), where operands are A (with binary representation $A_1A_{0(2)}$) and B (= $B_1B_{0(2)}$), and the product output is N (= $N_3N_2N_1N_{0(2)}$). Similar to the invertible logic gate implementation, a p-bit is assigned to each input and

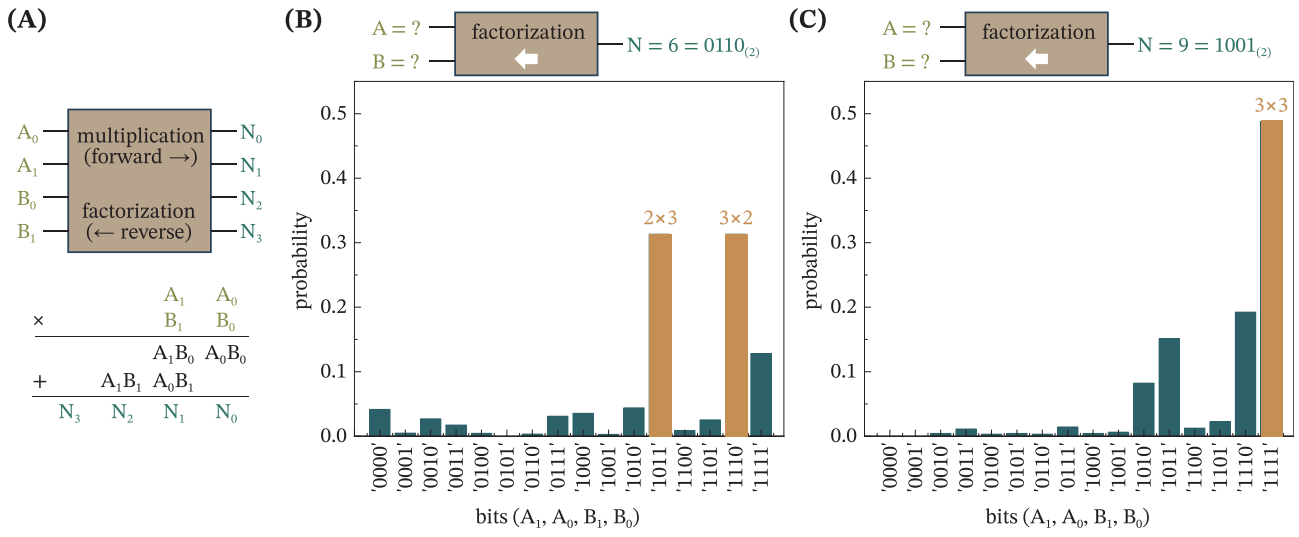


FIGURE 4 Integer factorization via p-bit network. (A) Configuration of 2-bit by 2-bit binary multiplier, where each digit of the operands (A and B) and the product (N) is represented by a p-bit, necessitating a total of 8 p-bits. (B) and (C) The factorization results, where the y-axis indicates the probability of each multiplicand combination predicted by the p-bit network across 500 feedback iterations. For product $N = 6$, the p-bit network correctly identifies the operands as 2×3 or 3×2 with a higher frequency than other combinations. Similarly, for a product $N = 9$, the p-bit network factorizes it as 3×3.

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output variable of the multiplier, requiring a total of 8 p-bits to configure a p-bit network. The energy function of this multiplier is defined as $E = (AB - N)^2$, which is further expanded in Equation (S6). The input functions for each p-bit are then derived by differentiating E, as summarized in Table S2.

Figure 4B,C presents the factorization results, showing the output probabilities obtained from each p-bit in the network over 500 cycles. For product $N = 6$, the most frequent output occurs when operands A and B are $10_{(2)}$ and $11_{(2)}$, or $11_{(2)}$ and $10_{(2)}$, respectively. This indicates that the p-bit network can factorize six as the product of two and three, or the product of three and two. Similarly, product $N = 9$ was successfully factorized as a product of 3 and 3, as shown in Figure 4C. Although this study demonstrates single-digit decimal factorization, the factorization capability of a p-bit network can be extended to larger digit numbers without altering the underlying principles.

The expansion of the demonstrated factorization capabilities has profound implications for the widely used RSA (Rivest-Shamir-Adleman) algorithm, which is predicated on the computational intractability of factoring large integers. For example, the RSA-2048 standard uses a 617-digit modulus formed by the product of two prime numbers, each approximately 100 digits in length. In the binary representation, the modulus comprises up to 2050 bits, with each prime factor containing approximately 333 bits. Therefore, a p-bit network comprising 2716 p-bits can theoretically factorize the RSA-2048 modulus. Given the high integrability of our p-bits with contemporary device technologies, it is anticipated that achieving the required p-bit density will be feasible. Moreover, unlike quantum computers, p-bit networks do not require cryogenic environments, potentially offering superior energy efficiency for a variety of combinatorial optimization tasks beyond the scope of the integer factorization examined in this study.

3 | CONCLUSION

This study demonstrates a novel p-bit device constructed using h-BN and SnS_2 nanosheets, exhibiting significant advancements in durability and energy efficiency for p-computing. By leveraging electron trapping and detrapping processes at the h-BN/SnS_2 interface, our p-bit achieves robust probabilistic switching over 10^8 cycles with minimal energy consumption. Integrating an active switch to mitigate static power consumption further enhances energy efficiency. Additionally, the innovative use of the pulse width for controlling probabilistic switching significantly improves noise immunity, thereby addressing a critical limitation of existing p-bit designs. Furthermore, we validate the practical applicability of our p-bit by implementing invertible Boolean logic gates and demonstrating integer factorization. These examples underscore the potential of a p-bit network to efficiently solve complex combinatorial optimization problems with significant implications for cryptographic applications such as RSA. The high integrability and low-power operation of p-bit networks offer a promising alternative to quantum computing solutions that require cryogenic environments. Consequently, our p-bit configuration has the potential to revolutionize the field of p-computing, opening new possibilities for energy-efficient solutions to complex problems.

While our findings suggest that the h-BN/SnS_2 material system offers intrinsic advantages for p-bit implementation, definitive experimental validation remains an open challenge. Our interpretation, primarily based on observed device behavior and energy band diagram analysis, supports the hypothesis that interface trap density plays a critical role in the probabilistic switching mechanism. However, further studies—such as spectroscopic analysis of interface states or comparative investigations with alternative 2D materials—are necessary to provide direct experimental evidence. Additionally, materials with lower interface trap density or wider band gaps than SnS_2 may enhance stability in probabilistic switching, warranting further exploration of alternative material combinations to optimize p-bit performance.

Given that prior p-bit studies have not employed 2D materials or carrier trapping mechanisms, our work provides new insights into material selection strategies for probabilistic computing. While our approach represents a novel and previously unreported attempt at implementing p-bit devices with 2D materials, additional experimental validation is essential to fully establish the advantages of the h-BN/SnS_2 system. We hope that our findings will serve as a foundation for future research, inspiring further exploration of 2D material-based probabilistic computing architectures.

4 | EXPERIMENTAL METHODS

4.1 | Fabrication of the p-bit and active switch

The devices were fabricated on a heavily n-doped Si wafer substrate. A 40-nm-thick film of Al_2O_3 was deposited on the substrate by atomic layer deposition at 350°C, using N_2 as the carrier gas at a pressure of 1.0 Torr. $Al(CH_3)_3$ (TMA) and H_2O were introduced into the carrier gas flow, resulting in a final pressure increase of 1.1 Torr. The growth rate of the Al_2O_3 layer was

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approximately 1 Å/cycle. Subsequently, to prepare the SnS_2 nanosheets, we mechanically exfoliated bulk SnS_2 (supplied by HQ Graphene) using sticky Scotch tape. After exfoliation, the tape was adhered to a polydimethylsiloxane (PDMS) stamp and transferred onto the target Al_2O_3/Si substrate using a dry transfer method with a microaligner. Subsequently, we patterned the source and drain electrodes using electron-beam lithography and deposited Ti/Au (10 nm/50 nm) at rates of 0.5 and 1.5 Å/sec, respectively, in a thermal evaporation chamber operating at 1.1×10^{-7} torr. The lift-off process was accomplished by immersion in acetone for 3–4 h, followed by washing with methanol and finally drying using a N_2 gas blow. The h-BN flakes were then transferred to the top of the SnS_2 flake using a microaligner tool with a PDMS stamp. The patterning of the gate electrode was then repeated using electron-beam lithography, followed by the deposition of Ti/Au (10 nm/100 nm). Finally, another lift-off process was performed.

4.2 | Electrical measurement

All the pulses were applied to the gate and drain electrodes using a function generator (Keysight 33622a). The drain current was then measured through the source electrode in real time using a current waveform analyzer (Keysight CX3324a). All the device measurements were performed at room temperature in ambient air within a shielded dark box.

4.3 | p-bit model

The input–output characteristics of our p-bit fit well to a sigmoid function, as shown in Figure 3C, allowing the output of the p-bit (p_i) to be modeled as a function of a dimensionless input function I_i:

$$p_i = U[\sigma(I_i) - r], \tag{5}$$

where σ is the sigmoid function, and U is the step function ensuring the output is either 0 or 1. Crucially, r is a random variable that introduces stochasticity to p_i, corresponding directly to the mean and standard deviation values obtained from Figure 3C. These parameters were explicitly incorporated into our model to ensure an accurate representation of the probabilistic behavior observed experimentally.

In the theoretical framework of p-computing detailed in Supporting Information Note 3–1, p_i is originally defined as either -1 or $+1$. However, to maintain consistency with the common digital bits, a step function was used instead of the sign function in Equation (4), resulting in p_i values of either 0 or 1. Subsequently, because the physical input variable in our p-bit is t_{pulse}, I_i is mapped to t_{pulse} as:

$$p_i = U\left[\sigma\left(\frac{t_{pulse} - t_0}{t_s}\right) - r\right], \tag{6}$$

where t_0 is the offset pulse width corresponding to a 50% probability of π being 1, and t_s is the fitting parameter. In the simulation, t_0 of 291 μs and t_s of 1.62 s were used.

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CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

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