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A 5 Gb/s Optoelectronic Receiver IC in 180 nm CMOS for Short-Distance Optical Interconnects

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Abstract: This paper presents a CMOS-based optoelectronic receiver integrated circuit (CORIC) realized in a standard 180 nm CMOS technology for the applications of short-distance optical interconnects. The CORIC comprises a spatially modulated P^+/N-well on-chip avalanche photodiode (P^+/NW APD) for optical-to-electrical conversion, a dummy APD at the differential input for enhanced common-mode noise rejection, a cross-coupled differential transimpedance amplifier (CCD-TIA) for current-to-voltage conversion, a 3-bit continuous-time linear equalizer (CTLE) for adaptive equalization by using NMOS registers, and a f_T-doubler output buffer (OB). The CTLE and f_T-doubler OB combination not only compensates the frequency-dependent signal loss, but also provides symmetric differential output signals. Post-layout simulations of the proposed CORIC reveal a transimpedance gain of 53.2 dBΩ, a bandwidth of 4.83 GHz even with a 490 fF parasitic capacitance from the on-chip P^+/NW APD, a dynamic range of 60 dB that handles the input photocurrents from 1 μA_{pp} to 1 mA_{pp}, and a DC power consumption of 33.7 mW from a 1.8 V supply. The CORIC chip core occupies an area of 260 × 101 μm^2.

Keywords: APD; CTLE; f_T-doubler; optoelectronic; TIA

1. Introduction

The growing demand for high-speed, energy-efficient data communication has led to significant advancements in CMOS-based optoelectronic receivers, particularly targeting short-distance optical interconnect applications [1]. These interconnects, which leverage the advantages of optical signaling—such as wide bandwidth and low latency—are increasingly being deployed in environments requiring high data throughput and reliability, including data centers, high-performance computing (HPC) clusters, and server farms [2,3]. Compared to traditional electrical links, optical interconnects offer superior scalability in terms of bandwidth density and energy efficiency, which are essential for meeting the demands of next-generation computing workloads.

Recent research efforts have focused on integrating photodetectors with an analog front-end circuitry in a single CMOS chip to enhance bandwidth and reduce power consumption simultaneously [4–7]. These monolithic solutions eliminate the need for discrete optical components and reduce the parasitic effects introduced by the unavoidable interconnect and packaging, thereby enabling compact, cost-effective implementations. Particularly, co-design strategies involving on-chip photodetectors and equalization circuits such as CTLEs have demonstrated promise in extending the data rate while maintaining low power budgets [8]. However, realizing such designs in a standard CMOS process without compromising noise performance, signal integrity, and linearity poses severe circuit-level challenges.

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In this paper, we propose a novel optoelectronic receiver architecture optimized for short-range optical interconnects, called 'CMOS-based optoelectronic receiver integrated circuit (CORIC)', which comprises an on-chip avalanche photodiode (APD), a cross-coupled differential transimpedance amplifier (CCD-TIA), a 3-bit programmable continuous-time linear equalizer (CTLE), and an f_T-doubler, as shown in Figure 1. In particular, the CCD-TIA employs cross-coupled active loads that enhance the gain and stabilize the output swing while providing low input-referred noise and efficient current-to-voltage conversion [9]. The CTLE dynamically compensates for the channel-induced frequency-dependent losses by adaptively tuning its resistance (Rs) and capacitance (Cs), thereby preserving the signal fidelity across varying operating conditions. In addition, the f_T-doubler serves as a high-bandwidth output buffer (OB), hence boosting the circuit's overall drive capability for subsequent digital processing blocks.

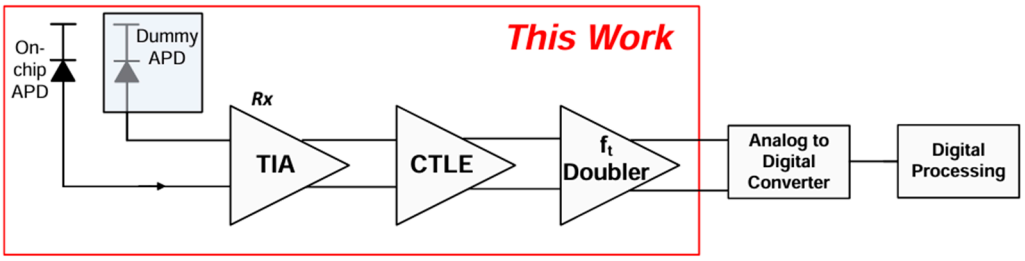


Figure 1. Block diagram of the proposed CORIC.

Conventional optical receivers mostly rely on external photodiodes—either p-i-n photodiodes or APDs—which necessitate off-chip interconnects using bond wires and include integrated electrostatic discharge (ESD) protection circuits. However, these external components introduce significant parasitic inductance and capacitance, which not only restrict the achievable bandwidth, but also degrade the overall signal-to-noise ratio (SNR) and thus increase jitter. Moreover, the use of discrete APDs significantly raises the packaging complexity and cost especially for multi-channel optical array systems where high integration density is critical. To alleviate these limitations, this work integrates on-chip APDs in a standard 180 nm CMOS platform, hence eliminating the need for external optical detectors and their associated parasitic elements. This monolithic integration strategy simplifies the receiver architecture, and also enhances the performance metrics such as bandwidth, noise efficiency, and cost per channel, making it highly suitable for scalable optical interconnect solutions.

2. Circuit Description

2.1. On-Chip P⁺/NW APD

On-chip APDs are fabricated by using a 180 nm CMOS process. Figure 2 illustrates the cross-sectional view of the fabricated on-chip APD, which shares the same configuration as the P⁺/N-well (NW) APD reported in [10].

Figure 3a depicts the current–voltage characteristics of the fabricated on-chip CMOS P⁺/NW APD, measured under both dark and illuminated conditions. A notable increase in both dark and photocurrent is observed near the breakdown voltage of 11.1 V, which is attributed to the avalanche multiplication effects. These measurements were performed with an incident optical power of approximately –60 dBm. The responsivity R of the APD is calculated by using the following expression:

$$R = \frac{I_{Illumination} - I_{dark}}{P_{opt}},$$

where $I_{Illumination}$ and I_{dark} denote the measured currents with and without optical input, and P_{opt} is the optical power incident on the device.

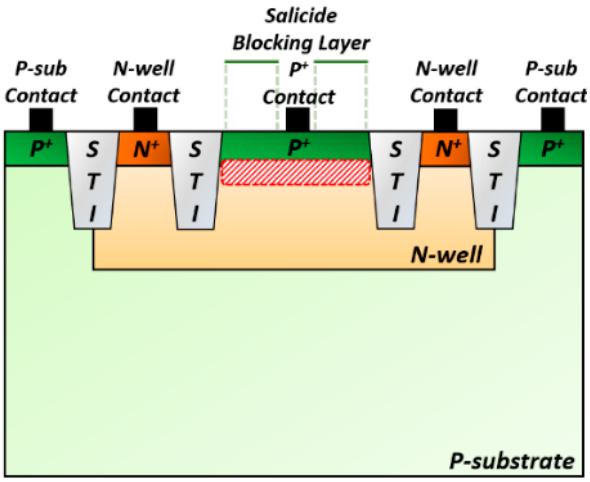
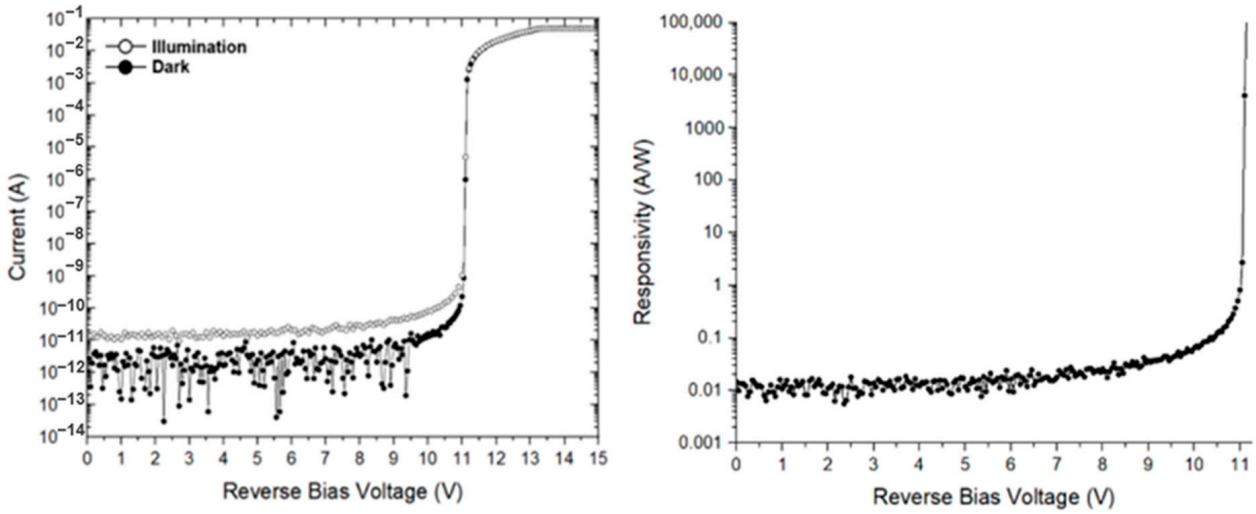


Figure 2. Cross-sectional view of the on-chip P$^+$/N-well APD.



(**a**) (**b**)

Figure 3. Measured (**a**) current and (**b**) responsivity of on-chip P$^+$/NW APD at reverse bias voltages [10].

Figure 3b presents the variation of responsivity with respect to the reverse bias voltages, showing that a peak responsivity of 2.72 A/W is achieved at 11.05 V [10]. The on-chip P$^+$/NW APDs are designed with an octagonal shape to prevent premature edge breakdown with a diagonal length of 40 μm in the optical window [11], which results in a parasitic capacitance of 0.49 pF.

2.2. Cross-Coupled Differential Transimpedance Amplifier (CCD-TIA)

Figure 4 shows the schematic diagram of the cross-coupled differential transimpedance amplifier (CCD-TIA), in which cross-coupled active loads comprising PMOS loads (M3, M4) and NMOS source-followers (M5 with R1 and M6 with R2) are employed. Since the gates of the active loads are cross-connected, symmetric differential outputs can be generated at the output nodes of the CCD-TIA, not to mention that the bandwidth performance can be enhanced.

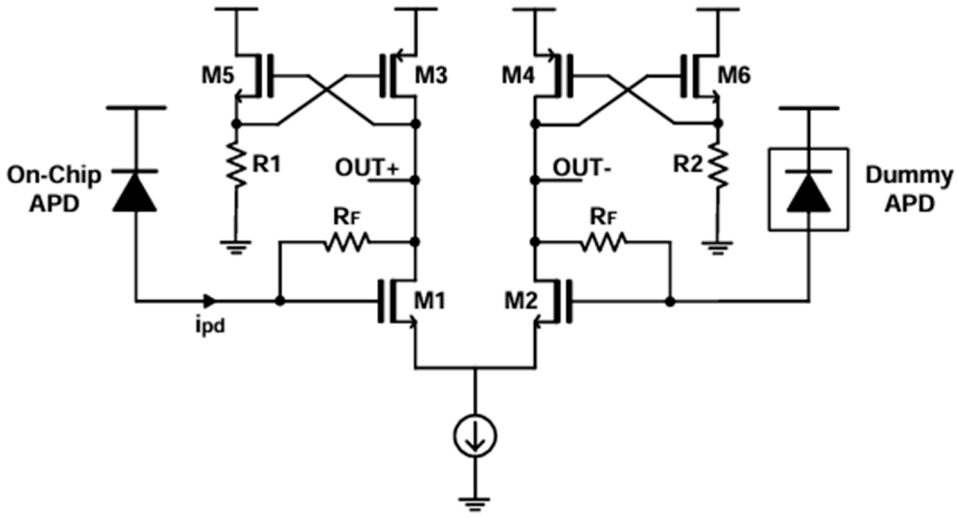


Figure 4. Schematic diagram of the CCD-TIA.

When light pulses are absorbed by the on-chip APD, the optical signals are converted into electrical currents (i_{pd}) that flow to the gate of M1. A variable feedback resistor (R_F) is positioned between the input and output nodes, providing negative feedback operations. Using small-signal analysis, the transimpedance gain for this CCD-TIA can be given by

$$\frac{v_o^+}{i_{pd}} \cong \frac{R_F g_{m1}}{g_{m1} + g_{m3}} \cong R_F \; if \; g_{m1} \gg g_{m3}$$

$$\frac{v_o^-}{i_{pd}} \cong -\frac{R_F g_{m1}}{g_{m1} + g_{m3}} \cong -R_F \; if \; g_{m1} \gg g_{m3},$$

where $g_{mi(i = 1,3,5)}$ denotes the transconductance of transistor $M_{i(i = 1,3,5)}$.

Also, the equivalent noise current spectral density of the CCD-TIA is given by

$$\overline{I_{eq}^2} \cong \frac{4kT}{R_F} + \left(\frac{4kT\Gamma g_{m1} + 4kT\Gamma g_{m3}}{g_{m1}^2}\right)\left(\frac{1}{R_F^2} + \omega^2 C_{tot}^2\right) + \left(\frac{4kT\Gamma g_{m5} + \frac{4kT}{R_1}}{g_{m5}^2 R_F^2}\right) \cong \frac{4kT}{R_F} + \frac{4kT\Gamma(g_{m1} + g_{m3})\omega^2 C_{tot}^2}{g_{m1}^2},$$

where C_{tot} represents the total input capacitance including the photodiode capacitance (C_{pd}) and the gate capacitance of M1. Therefore, this analysis reveals that enlarging g_{m1} and g_{m5} while minimizing g_{m3} can be essential to obtain low noise performance.

2.3. 3-Bit Continuous-Time Linear Equalizer (CTLE)

A 3-bit continuous-time linear equalizer (CTLE), illustrated in Figure 5, is utilized to achieve adaptive equalization through the integration of advanced techniques such as source degeneration, inductive peaking, and negative capacitance [12]. These techniques strategically shape the transfer function by introducing a programmable zero-pole pair, which enhances the high-frequency gain and compensates for the frequency-dependent loss of the preceding channel. Specifically, inductive peaking extends the bandwidth by mitigating the effect of the dominant pole, while negative capacitance cancels parasitic capacitance to maintain gain at higher frequencies. The CTLE operates in a fully analog manner without requiring any clock signal, making it suitable for high-speed, low-power applications.

To enable dynamic adaptation to varying channel conditions, a 3-bit digital-to-analog converter (DAC) is incorporated to control the NMOS resistor array used for source degen-

eration. In conjunction with programmable capacitors, the DAC adjusts Rs and Cs values in real time, allowing the CTLE to autonomously tune its gain and bandwidth. This results in a fully adaptive equalization mechanism that optimizes signal integrity across different levels of inter-symbol interference (ISI) and channel attenuation [13].

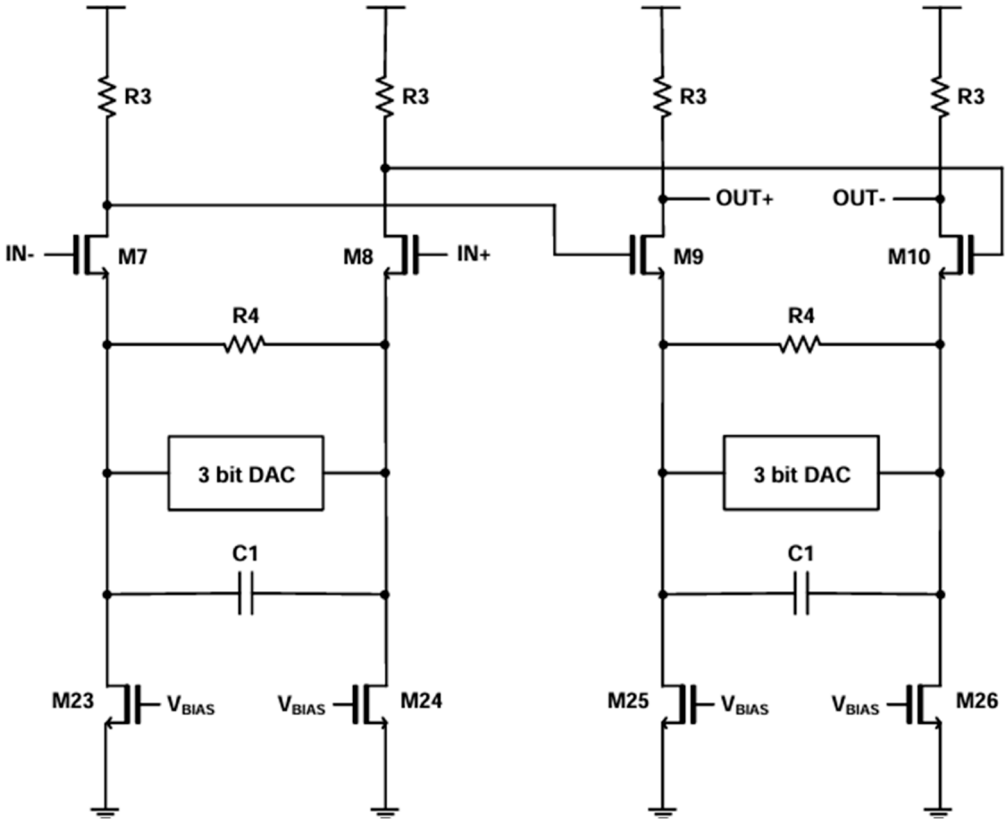


Figure 5. Schematic diagram of the 3-bit CTLE.

In terms of noise performance, the CTLE introduces thermal noise primarily from the source degeneration resistor and the active devices in the signal path. While inductive peaking and negative capacitance improve bandwidth, they may also contribute additional noise or affect noise shaping depending on the design topology. Careful optimization of the resistor values and device sizing is required to minimize the overall input-referred noise and maintain a high signal-to-noise ratio (SNR), especially at high frequencies.

The input-referred noise voltage density can be approximated as

$$\overline{v}^2_{n,in} \approx 8kTRs + \frac{8kT\gamma}{g_{m7}} + \frac{8kT\gamma}{g_{m8}}$$

The input dynamic range of the CTLE is defined as the range of input voltage swings for which the circuit remains in its linear operating region. This can be expressed in terms of the Input Referred 1 dB Compression Point ($V_{in,1dB}$), beyond which the gain drops by 1 dB due to nonlinearity.

A rough estimate of the maximum linear input swing ($V_{in,max}$) for a differential input pair with source degeneration is given by

$$V_{in,max} \approx \frac{2I_{bias}\left(R_s + \frac{1}{g_{m7}}\right)}{\sqrt{2}}$$

This shows that adding source degeneration increases the linear input range, at the cost of reduced transconductance and possibly lower gain. Therefore, R_S and g_{m7} must be co-optimized to balance linearity, gain, and noise.

The filter's transfer function incorporating the capacitive degeneration can be given by

$$H(s) \cong \left(\frac{g_{m7} R_L}{1 + \frac{g_{m7} R_L}{2}} \cdot \frac{1 + \frac{s}{\omega_z}}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)} \right)^2,$$

where $\omega_z = \frac{1}{R_s C_S}, \omega_{p1} = \frac{1 + \frac{g_{m7} R_s}{2}}{R_s C_s}$, and $\omega_{p2} = \frac{1}{R_L C_L}$ [13].

2.4. f_T -Doubler

The f_T-doubler, often implemented by using a differential input stage with cross-coupled feedback or stacked transistors, is designed to extend the bandwidth of the amplifier by effectively doubling the transition frequency f_T. However, this improvement in speed and gain–bandwidth product comes with tradeoffs in terms of noise and linearity.

From a noise perspective, the input-referred noise voltage density $\overline{v}^2_{n,in}$ is primarily determined by the thermal noise contributions from both the input and feedback transistors. Assuming a stacked configuration with transistors M_{11} and M_{12}, the total input-referred noise can be approximated as

$$\overline{v}^2_{n,in} \approx \frac{8kT\gamma}{g_{m11}} + \frac{8kT\gamma}{g_{m12}},$$

where g_{m11} and g_{m12} are the transconductances of the input and feedback transistors, respectively, and γ is the MOSFET excess noise factor. Since both transistors contribute significantly to the noise, careful sizing and biasing are required to minimize $\overline{v}^2_{n,in}$ without compromising bandwidth.

The input dynamic range of the f_T-doubler is limited by the increased gain and potential instability introduced by positive feedback or stacking. The maximum linear input swing $V_{in,max}$ can be estimated as

$$V_{in,max} \approx \frac{V_{ov}}{1 - A_{fb}},$$

where V_{ov} is the overdrive voltage and A_{fb} is the effective feedback gain. A_{fb} approaches unity, the input range narrows, and the circuit may enter a non-linear or unstable regime. Thus, the feedback strength must be optimized to ensure a sufficient linear range while achieving the desired bandwidth.

An additional benefit of the f_T-doubler lies in its reduced input capacitance. As depicted in Figure 6, the gate–source capacitances C_{gs11} and C_{gs12} of the stacked transistors M_{11} and M_{12} appear in series from the input perspective. Assuming identical transistor sizes, the effective input capacitance becomes

$$C_{in,eff} \approx \frac{C_{gs11} \cdot C_{gs12}}{C_{gs11} + C_{gs12}} \approx \frac{C_{gs11}}{2}$$

This reduction in input capacitance contributes to an increase in the input pole frequency, further enhancing the overall bandwidth of the system.

Consequently, the cutoff frequency (f_T) for this f_T-doubler can be given by

$$\mathrm{f_t} \equiv \frac{\mathrm{g_{m11}}}{2\pi \mathrm{C_{gs11}}} \approx \frac{2\mathrm{g_{m11}}}{2\pi \mathrm{C_{gs11}}},$$

which demonstrates its capability to extend the bandwidth [14].

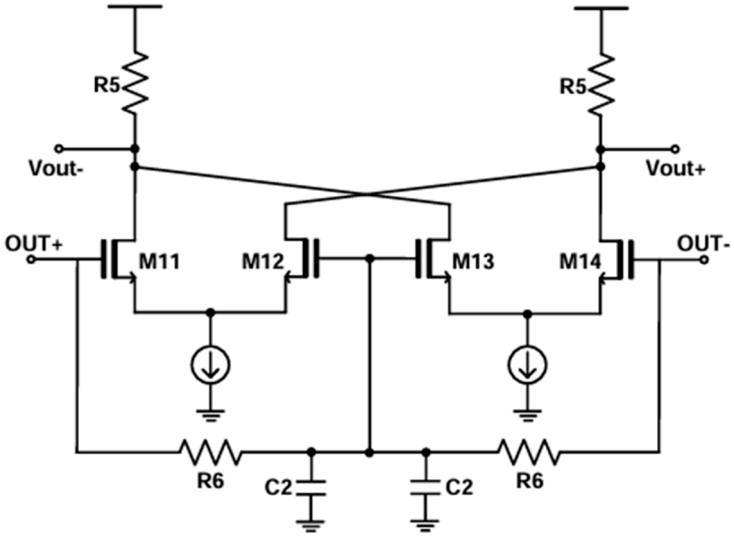


Figure 6. Schematic diagram of the f_T-doubler.

In addition, this f_T-doubler functions as an output buffer, providing a sufficient drive capability for subsequent stages while maintaining the symmetry of differential outputs [15].

3. Chip Layout and Post Layout Simulation Results

Figure 7 presents the layout of the CORIC by using a cost-effective 180 nm CMOS process, incorporating two integrated P^+/N-well APDs. The upper APD, which is only the actual APD, functions as the light-receiving area, while the bottom APD (i.e., dummy APD) is shielded by a metal layer.

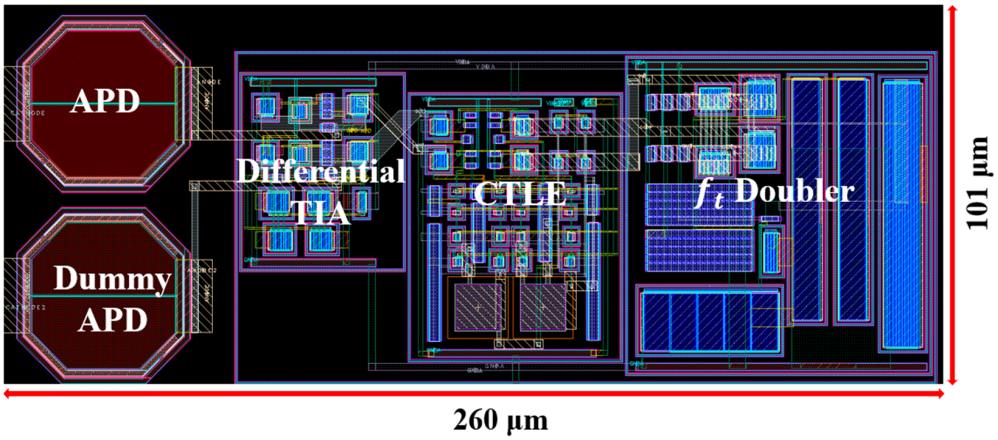


Figure 7. Layout of the proposed CORIC.

Consequently, incoming optical pulses are detected by the on-chip APD, which then converts them into photocurrent signals. The chip area is 260 × 101 μm², and the DC analysis indicates a power consumption of 33.7 mW from a 1.8 V supply.

Figure 8 illustrates the simulated frequency response of the CORIC, revealing a transimpedance gain of 53.2 dBΩ and a −3 dB bandwidth of 4.83 GHz. The simulation was conducted with the input capacitance set to 490 fF. Notably, a 3 dB peaking is observed near the bandwidth, which might be attributed to the inductive peaking effect introduced by the cross-coupled active loads.

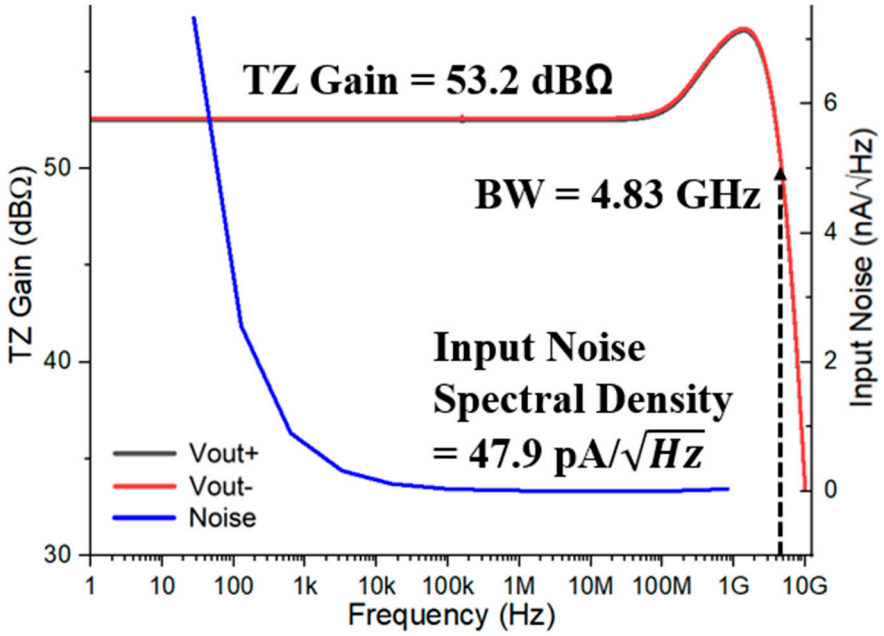


Figure 8. Simulated frequency response of the proposed CORIC.

Also, a high bandwidth can be acquired by using the CTLE and the f_T-doubler. Furthermore, the CORIC achieves an average noise current spectral density of 47.9 pA/$\sqrt{\text{Hz}}$ within the bandwidth, which corresponds to the optical input sensitivity of -25.9 dBm for a 10^{-12} bit-error-rate (BER) with the assumption of 2.72 A/W APD responsivity [10].

Figure 9 presents the simulated eye diagrams of the proposed CORIC for an input current of 300 μA_{pp} at various data rates of 1 Gb/s and 3 Gb/s, respectively. These results clearly demonstrate that the output amplitudes of the eye diagrams remain consistent across all data rates.

Figure 10 shows the simulated pulse response of the CORIC for the input currents ranging from 1 μA_{pp} to 1 mA_{pp}. These results confirm that the CORIC achieves an input dynamic range of 60 dB, especially with the aid of a 3-bit DAC gain control mechanism in the CTLE. Also, employing f_T-doubler not only enables the DC offset cancellation at the output nodes, but also ensures symmetric output signals [15]. Consequently, nearly identical amplitudes are achieved at the differential output pulses.

Table 1 compares the performance of the proposed CORIC with prior arts. Ref. [16] introduced a preamplifier based on a regulated cascode (RGC) circuit, combined with a single-to-differential (S/D) circuit, a DC-offset cancellation circuit, and an output buffer. Compared to the proposed CORIC, this preamplifier demonstrated a narrower transimpedance gain-to-bandwidth ratio and occupied a larger chip area despite the photodiode being off-chip.

Ref. [17] presented a common source (CS) amplifier with active inductive peaking (AP-TIA), followed by a post amplifier and an output driver. While implemented in a 130 nm process, this design showed a narrower transimpedance gain-to-bandwidth ratio and higher power dissipation per channel than the proposed CORIC system.

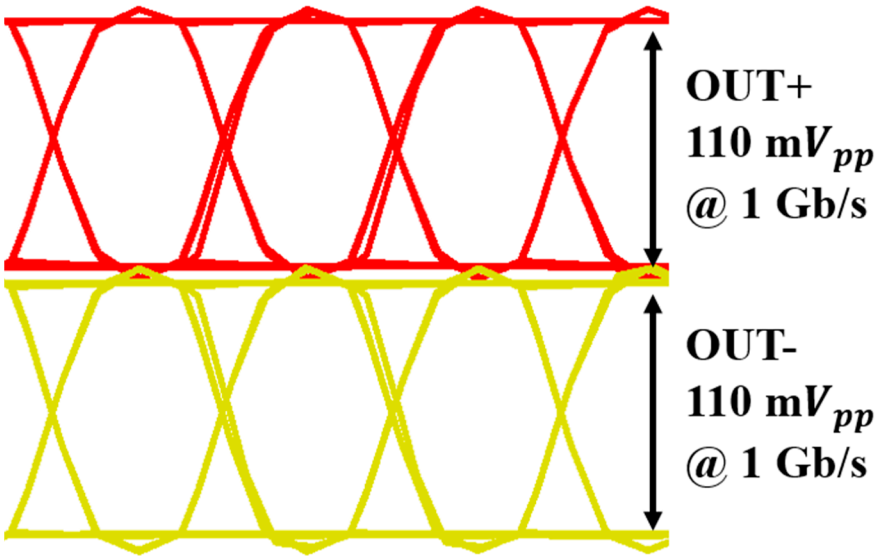
Ref. [18] suggested an inverter-based amplifier paired with an AC-coupled noise-cancellation circuit, along with a single to differential (S/D) and offset cancellation (OC) circuits. Even with a 40 nm process, the power dissipation per channel and chip area of this system exceeded those of the proposed CORIC.

Ref. [19] proposed a distributed amplifier featuring simple shunt peaking with additional inductor/transformer peaking in a common source (CS) stage. This system exhibited a narrower transimpedance gain-to-bandwidth ratio compared to the proposed design,

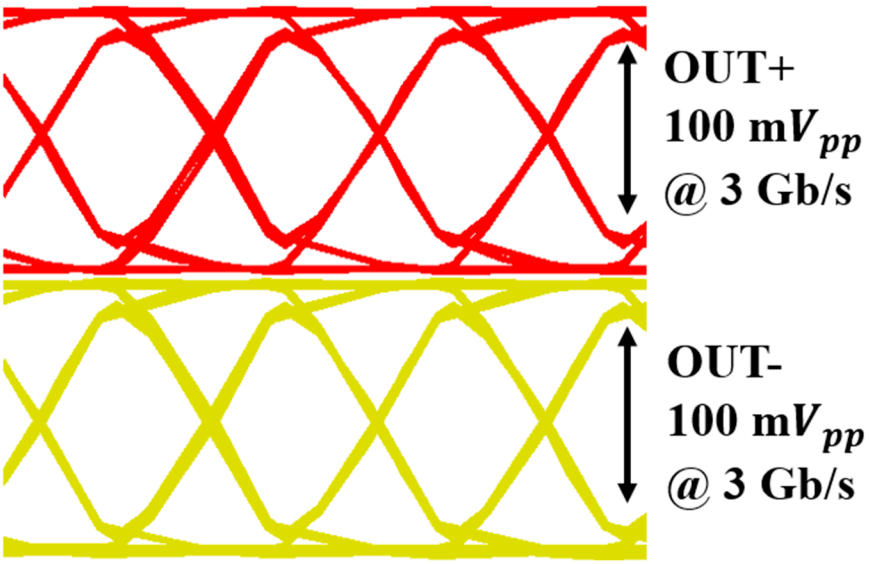
and its TIA required multiple supply voltages (1.5 V and 3.0 V), complicating the power supply design.

Ref. [20] realized a system composed of an under-damped TIA, a low-pass filter, and an output buffer. Although implemented in a 65 nm process, its chip area showed a minimal difference from that of the proposed CORIC system.

Hence, when compared to prior arts, the proposed CORIC provides competitive performance in terms of the gain-bandwidth tradeoff, despite its implementation in a relatively low-cost 180 nm CMOS process. While most state-of-the-art designs rely on advanced nodes (including 130 nm, 65 nm, or even 40 nm technologies) to achieve high performance, the CORIC demonstrates comparable performance with careful analog front-end architecture and circuit-level optimization—such as the use of a cross-coupled differential TIA and an adaptive equalizer. Namely, it attains comparable or even superior bandwidth and gain characteristics, which not only reduces the fabrication costs, but also enhances the circuit robustness and yield.



(**a**)



(**b**)

Figure 9. Simulated eye diagrams of the CORIC for 300 μA_{pp} input currents at different date rates of (**a**) 1 Gb/s and (**b**) 3 Gb/s, respectively.

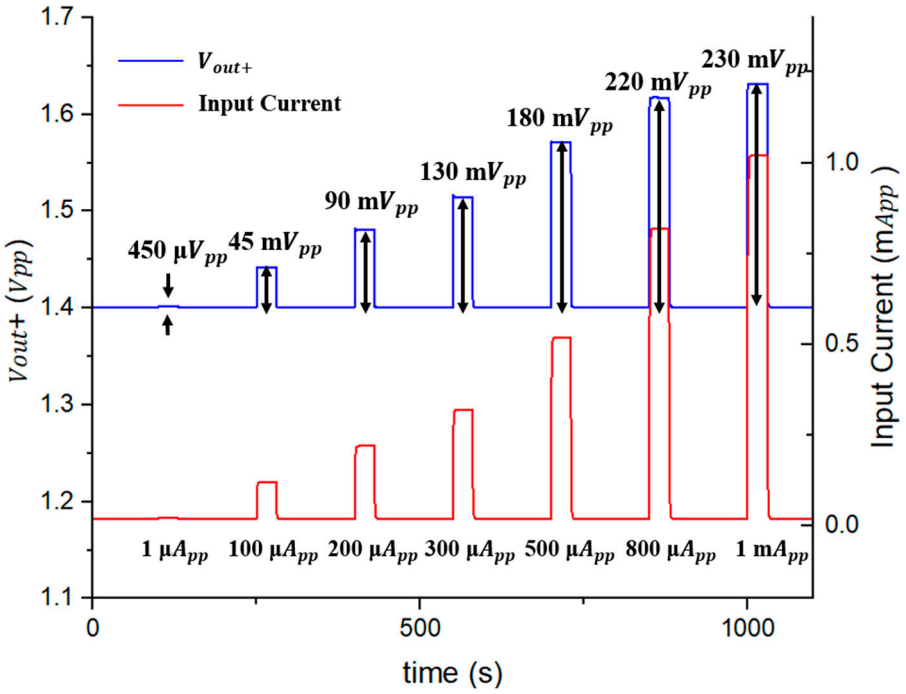


Figure 10. Simulated output pulses of the CORIC for different input currents.

Table 1. Performance comparison of the proposed CORIC with the recently published TIAs.

Parameters		[16]	[17]	[18]	[19]	[20]	**This work**
CMOS technology (nm)		180	130	40	180	65	180
PD	Type	Off-chip (Equiv. PD)	Off-chip (Equiv. PD)	Off-chip (Equiv. PD)	Off-chip (Equiv. PD)	On-chip (APD)	On-chip (APD)
	C_{pd} (pF)	0.5	2	0.2	0.22	-	0.5
	Responsivity (A/W)	-	1	-	-	-	2.72
	Wavelength (nm)	-	-	-	-	850	850
Input configuration		RGC	AP ‡	Diff.	CS ‡	Diff.	Diff.
Max. TZ gain (dBΩ)		72	76.8	64	54.5	60	53.2
Gain control		No	No	No	No	No	Yes
Bandwidth (GHz)		2.4	1.6	14.5	4.3	6.0	4.83
Input noise current density ($pA/\sqrt{Hz}$)		18.12	26.55	22.4	25.3	-	47.9
Dynamic range (dB)		-	-	-	-	-	60
Power dissipation per channel (mW)		§ 20.6 @ 1.8 V	47.3 @ 1.8 V	103 @ 1.2 V	§ 11.5 @ 1.5 V/3.0 V	§ 13.7 @ 1.2 V	33.7 @ 1.8 V
Chip area (mm^2)		0.173	§ 0.00035	1.1625	§ 0.0077	0.024	0.026

‡ Single-ended, § TIA only. RGC (regulated cascode), AP (active inductive peaking), Diff. (differential), CS (common source)

Moreover, the integration of an on-chip APD and a 3-bit programmable gain control mechanism enables the CORIC to achieve the dynamic range of 60 dB, which is particularly beneficial in scenarios with varying optical input power levels, such as multi-mode fiber

links or wavelength-division multiplexed systems. The on-chip APD eliminates the need for bulky off-chip photodetectors and their associated packaging and parasitic issues, thereby contributing to both area efficiency and noise reduction. In addition, the gain control allows the CORIC to adapt its amplification level according to input signal strength, ensuring consistent signal quality and preventing saturation under strong inputs while preserving sensitivity for weak signals.

This level of integration helps to minimize the overall chip area, and also contributes to a balanced power consumption profile, making the CORIC a well-rounded solution for compact, low-cost, and energy-efficient short-distance optical interconnects. Since many prior works exhibited limitations such as the requirements for multiple supply voltages, higher per-channel power consumption, or larger silicon area, despite being realized in more advanced technology nodes, the CORIC stands out by offering a practical and scalable solution that balances performance, integration, and power efficiency without relying on cutting-edge semiconductor processes.

4. Conclusions

We have presented a CMOS-based optoelectronic receiver integrated circuit (CORIC) optimized for short-distance optical interconnect applications. The proposed CORIC adopts a fully differential architecture with cross-coupled active loads, which significantly enhances the dynamic range while maintaining compactness and energy efficiency. Post-layout simulations by utilizing a standard 180 nm CMOS process verify the performance, showing a transimpedance gain of 53.2 dBΩ, a -3 dB bandwidth of 4.83 GHz, an input sensitivity of -25.9 dBm at a bit error rate (BER) of 10^{-12}, a wide dynamic range of 60 dB, and 33.7 mW power consumption from a single 1.8 V supply, hence demonstrating an excellent tradeoff between speed, gain, power, and integration. It is also noteworthy that achieving a 4.83 GHz bandwidth with a standard 180 nm CMOS process is particularly significant owing to the careful circuit-level optimization including cross-coupled loading. The high-frequency performance is further improved by incorporating a 3-bit continuous-time linear equalizer (CTLE) and an f_T-doubler. The CTLE adaptively compensates for the frequency-dependent losses that occur from PCB traces and interconnect parasitics, ensuring signal integrity across the entire bandwidth. The f_T-doubler operates as an output driver that extends the high-frequency response and provides robust differential drive strength for the subsequent digital processing stages. These features jointly contribute to the CORIC's suitability for high-speed optical communication systems, particularly in scenarios requiring strict power budgets and area constraints.

Conclusively, the proposed CORIC architecture provides academic contributions in the fields of high-speed analog/mixed-signal designs and exhibits strong industrial potential. The use of standard 180 nm CMOS technology makes the solution highly manufacturable and cost-efficient, especially when compared to advanced node implementations that require higher mask costs and present yield challenges. The low power consumption and small footprint of the design enable its integration into dense multi-channel transceiver modules, such as those used in optical interconnects within data centers, high-performance computing (HPC) systems, and next-generation optical backplanes. In addition, the monolithic integration of avalanche photodiodes (APDs) significantly simplifies the receiver architecture by eliminating the need for external photodiodes, wire bonding, and complex ESD protection networks. This not only reduces the system complexity and the packaging cost, but also improves the noise performance by minimizing the parasitic inductance and the capacitance. Such compact, scalable integration paves the way for single-chip optical front-end modules or full system-on-chip (SoC) optical transceivers, which are highly desirable in today's rapidly evolving data infrastructure.

Given the surging demand for energy-efficient, high-speed, and scalable optical I/O solutions, this work offers a viable and forward-looking receiver architecture. The presented CORIC could serve as a foundational building block in the development of future high-bandwidth, low-power optical communication systems for commercial, industrial, and even aerospace applications, where robustness, cost, and integration are of paramount importance.

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