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Advanced polynomial Y-function method for precise mobility characterization in 2D FETs

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Accurate extraction of mobility parameters in two-dimensional (2D) transition metal dichalcogenide (TMD)-based field-effect transistors (FETs) is crucial for evaluating their performance and optimizing device design. Conventional mobility extraction methods such as the field-effect mobility approach suffer from inaccuracies owing to the influence of series resistance and noise amplification. In this paper, we present an advanced polynomial Y-function methodology for the precise mobility characterization of MoS_2 FETs. This methodology enables a systematic discrimination among various scattering mechanisms while precisely extracting the threshold voltage. Through a comparative analysis of back-gate (BG) and top-gate (TG) MoS_2 FET configurations, we demonstrated the superior accuracy and consistency of the proposed method compared with conventional approaches. The results revealed that the TG-FET exhibited stronger surface-roughness scattering owing to the intensified transverse electric field from the thinner dielectric layer, leading to pronounced mobility degradation. The polynomial Y-function method successfully isolates key degradation factors, thereby enabling a more comprehensive understanding of the carrier transport mechanisms in 2D FETs. These findings provide a robust framework for optimizing 2D material-based electronic devices, facilitating their integration into next-generation nanoelectronic applications.

The advent of mechanical exfoliation techniques for obtaining atomically thin graphene has catalyzed the exploration and application of various two-dimensional (2D) materials[1]. These 2D materials are characterized by reduced dimensionality, a high surface-to-volume ratio, mechanical flexibility, and unique optical properties and have shown immense potential for various nanotechnological applications[2–5]. Among these, transition metal dichalcogenides (TMDs) have gained significance owing to their diverse range of electronic properties, ranging from semiconducting to semi-metallic, metallic, and superconducting behavior[6,7]. This wide range of properties has made TMDs promising materials for technological advancement of the existing nanoelectronic devices.

Semiconducting TMDs, including MoS_2, $MoSe_2$, WS_2, and WSe_2, are particularly notable for their intrinsic bandgaps, which are in stark contrast to the zero bandgap of graphene. This characteristic makes TMDs particularly promising channel materials for field-effect transistors (FETs). A significant advantage of TMDs is their ability to be scaled down to a monolayer thickness (0.6–0.7 nm) without compromising their semiconducting properties, thereby substantially enhancing FET performance. In contrast, conventional three-dimensional semiconductors encounter severe challenges at such reduced dimensions, predominantly owing to increased carrier scattering at the channel-to-dielectric interfaces, which severely degrades their carrier mobility[8]. Furthermore, the inherent absence of dangling bonds in TMDs results in superior channel-to-dielectric interfaces, further improving FET performance[8]. Consequently, TMD-based FETs (2D FETs) have garnered extensive attention because of their potential to outperform traditional silicon-based FETs. Recent studies have demonstrated the feasibility of fabricating complex electronic components using 2D FETs, including microprocessors[9], operational amplifiers[10], and SRAM cells[11].

Mobility is a critical parameter for evaluating FET performance because it directly affects the current-carrying capability and switching speed of the device. Theoretical estimates based on density functional theory provide the intrinsic mobility for semiconducting TMDs. For example, MoS_2 has an intrinsic mobility (μ_0) of approximately 270 $cm^2V^{-1}s^{-1}$[12]. However, the experimental field-effect mobilities (μ_{FE}) observed in MoS_2-based FETs are significantly lower, generally in the 30–60 $cm^2V^{-1}s^{-1}$ range, as summarized in Supporting Table S1. This significant discrepancy highlights the impact of various scattering mechanisms, including phonon scattering from dielectrics, Coulomb scattering from charge impurities, defect-induced scattering, and interfacial surface

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roughness[13]. Therefore, a thorough analysis of these scattering mechanisms is essential to accurately assess the mobility and performance potential of 2D FETs.

Specifically, these scattering effects are predominantly influenced by the transverse electric field from the gate, making the following factors crucial determinants of mobility: thickness and permittivity of the gate dielectric and the channel thickness[14]. However, as indicated in Supporting Table S1, changes in the gate dielectric or MoS_2 thickness did not exhibit a consistent impact on the μ_{FE}. This inconsistency is largely attributed to the methodology used for extracting μ_{FE}. Typically, μ_{FE} is derived from the transfer characteristic (drain current versus gate voltage characteristic, I_D–V_G) and its differentiation (transconductance, $g_m=\partial I_D/\partial V_G$) in the FET's linear region. This can be expressed as:

$$I_D = \frac{W}{L}\mu_{FE}C_{ox}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \tag{1}$$

$$\mu_{FE} = \frac{dI_D}{dV_G}\frac{L}{WC_{ox}V_D} = g_m\frac{L}{WC_{ox}V_D} \tag{2}$$

where L and W denote the channel length and width, respectively, C_{ox} is the gate dielectric capacitance per unit area, and V_T and V_D denote the threshold voltage and drain bias, respectively, with the source bias (V_S) assumed to be grounded. However, this approach is prone to inaccuracies owing to the influence of series resistance (R_s), which can distort the measured I_D values. Moreover, the differentiation process used to obtain g_m tends to amplify the measurement noise, further propagating errors into the extracted μ_{FE}. Furthermore, the inaccuracy in the extracted μ_{FE} is exacerbated by the arbitrary selection of the V_G range for linear regression when determining g_m. Therefore, an accurate mobility extraction methodology should be employed to minimize, or potentially eliminate, the effects of R_s and its dependence on the arbitrary choice of the V_G range.

In this study, we present an advanced polynomial Y-function method designed for the precise extraction of mobility parameters in 2D FETs, improving upon existing approaches by accurately distinguishing between various scattering mechanisms and enabling the simultaneous extraction of the threshold voltage. MoS_2 was chosen as the model material because it is the most extensively studied among semiconducting TMDs, offering a rich accumulation of experimental results and literature data. This extensive background provides a robust foundation for benchmarking the proposed extraction methodology. Through a comparative analysis of mobilities extracted from MoS_2 FETs with both back-gate (BG) and top-gate (TG) configurations, we identified and corrected the inaccuracies present in previously reported mobility values. Our results demonstrate the enhanced precision and reliability of the proposed method, establishing it as a robust tool for characterizing the transport properties of 2D FETs.

Background of Y-function method

The Y-function method was developed to provide a more accurate extraction of the mobility parameters[15]. The theoretical basis of the Y-function method is detailed in Supporting Notes 1.1 and 1.2. The Y-function is defined in the linear region of the FET with a very low V_D. It is expressed as:

$$Y \equiv \frac{I_D}{\sqrt{g_m}} = \sqrt{G_m}V_{Gt} \tag{3}$$

where $G_m = (W/L)\mu_0 C_{ox} V_D$ is the static transconductance, and $V_{Gt} = V_G - V_T - V_D/2$ represents the effective gate drive voltage. This method leverages the fact that I_D and g_m are similarly affected by R_s, allowing the Y-function to minimize the impact of R_s on the extracted mobility. Equation (3) implies that the linear regression of the Y-function against V_{Gt} facilitates the extraction of V_T and G_m, which are identified as the x-axis intercept and slope of the regression line, respectively. Once G_m is determined, μ_0 can be calculated using known values of W, L, C_{ox}, and V_D.

Furthermore, the Y-function method can isolate the effects of various scattering mechanisms on the mobility by differentiating between phonon scattering, surface roughness scattering, and Coulombic interactions. This is achieved through the extraction of specific attenuation factors, which quantify the impact of each scattering type on the mobility degradation, allowing for a more precise evaluation of the carrier transport properties in 2D FETs. Specifically, the scattering effects induced by the transverse electric field degrade mobility, making it dependent on V_{Gt}. To capture this dependency, μ_{FE} is typically modeled with a low-field mobility μ_0 and two attenuation factors θ_1 and θ_2 as:[16,17]

$$\mu_{FE} = \frac{\mu_0}{1 + \theta_1 V_{Gt} + \theta_2 (V_{Gt} - \Delta V_T)^2} \tag{4}$$

Here, θ_1 represents the contributions of phonon scattering and R_s on mobility degradation. Meanwhile, θ_2 accounts for field-enhanced interface-related scattering processes, particularly under higher transverse electric fields, with its onset shift captured by the term ΔV_T. It should be noted that, unlike conventional silicon MOSFETs, the atomically smooth van der Waals lattice of TMDs does not intrinsically exhibit surface roughness. Instead, θ_2 captures additional scattering mechanisms arising at the channel–dielectric interface, such as the effects of trapped charges, local interface inhomogeneities, or remote phonon interactions under strong gate fields. Therefore, when applying the Y-function method, the attenuation factors θ_1 and θ_2 should be interpreted as effective empirical parameters that represent the dominant but overlapping scattering contributions under different gate field conditions. These factors do not strictly isolate individual scattering mechanisms but rather

capture their combined influence. Coulomb scattering, while significant at low gate biases, is assumed to be effectively screened in the ON-state where the channel is fully conducting, and thus is not explicitly modeled. Additionally, the Y-function method is based on the drift-diffusion transport framework, and its validity is confined to regimes where carrier transport can be accurately described by drift and diffusion processes. Consequently, by extracting and analyzing these mobility parameters (μ_0, θ_1, θ_2, and ΔV_T), the Y-function method provides a comprehensive understanding of the physical mechanisms that influence mobility in 2D FETs. This semi-empirical analysis is critical for optimizing device performance and reliably interpreting the experimental data.

This Y-function method has been advanced significantly, enabling a more precise extraction of mobility parameters. Its basic variant[15], which operates under the assumption that $\theta_2 = 0$, allows extraction of only μ_0 and θ_1 (Supporting Note 1.2). However, this basic method is applicable only to FETs, where field-enhanced interface-related scattering processes are negligible. To overcome this limitation, more refined variants, including the direct[18] and Y-Φ methods[19], have been introduced to additionally account for θ_2 (Supporting Notes 1.3 and 1.4). The most sophisticated variant, the polynomial method[20], can extract all relevant mobility parameters through an iterative process (Supporting Note 1.5). To provide a clearer comparison of these mobility extraction methods, Table S3 summarizes their respective advantages, limitations, and suitable application conditions. This comparative overview will assist researchers in selecting an appropriate methodology based on device characteristics and measurement environments.

Despite these recent advancements, previous studies analyzing the mobility parameters of 2D FETs (Supporting Table S2) have exclusively employed the basic method, which is inherently unsuitable for 2D FETs because of the ultrathin nature of 2D materials. In these materials, the transverse electric field is intrinsically strong and is further intensified by high-k dielectrics or hexagonal boron nitride (h-BN) gate dielectrics, thereby exacerbating field-enhanced interface-related scattering. Consequently, neglecting θ_2 in these analyses introduces significant uncertainty in the extracted mobility parameters of 2D FETs.

Results and discussions

MoS_2 fets and their characterization

Figure 1a presents schematics and optical microscope images of MoS_2 FETs configured with both BG and TG structures. Both device architectures feature a gate length and channel width of 2 μm and 4.5 μm, respectively. The key distinction between these configurations lies in their gate dielectric layers: in the BG-FET, the underlying 300 nm-thick SiO_2 serves as the gate dielectric, whereas in the TG-FET, a 15 nm-thick Al_2O_3 layer deposited on top of the MoS_2 functions as the dielectric. Figure 1b shows the thickness measurements of each layer as determined using atomic force microscopy (AFM). Both the BG-FET and TG-FET were fabricated from MoS_2 flakes confirmed by AFM to have an identical thickness of 6.9 nm (approximately 10–11 layers), ensuring that any thickness-related variation in mobility extraction is minimized. Owing to the substantial difference in the dielectric thickness—300 nm for SiO_2 in the BG-FET versus 15 nm for Al_2O_3 in the TG-FET—the TG-FET was expected to experience a stronger transverse electric field, potentially leading to enhanced field-enhanced interface-related scattering.

Device characterization was performed using the multiple pulsed current–voltage (MPIV) method (Fig. 1c)[21]. In this setup, a pulse generator unit (PGU) applies V_G and V_D pulses with duration t_p, whereas a current waveform analyzer (CWA) captures the resulting drain current (I_D) through the source electrode in real time. This technique minimizes the measurement-induced degradation by reducing the gate biasing period, thereby preserving the intrinsic electrical characteristics of the device. Notably, when the transfer characteristics of the BG-FET were measured using only a source measurement unit (SMU) under a DC bias, clockwise hysteresis was observed even under vacuum conditions (Fig. 1d). This was possibly a result of DC bias-induced stress. In contrast, the MPIV method, with t_p = 1 μs, eliminated hysteresis effects (Fig. 1e), indicating its effectiveness in mitigating bias stress. Although the MPIV method is limited by the noise bandwidth of the CWA, which prevents the measurement of I_D below 1 nA, it does not affect the extraction of mobility parameters via the Y-function method, which relies only on data from the ON-state region. Consequently, all subsequent analyses presented in this paper were conducted using the MPIV method.

Mobility parameters in BG-FET

In this section, we analyze the mobility parameters of the BG-FET extracted using both basic[15] and polynomial[20] Y-function methods. The basic Y-function method begins with the simplest drain current model, given by

$$I_D = G_m \frac{V_{Gt}}{1 + \theta_1 V_{Gt}} \tag{5}$$

The Y-function was constructed by applying Eq. (3) to the transfer characteristics shown in Fig. 1e. Figure 2a shows the Y-function as a function of V_G, where the slope and x-axis intercept correspond to G_m and V_T, respectively. However, owing to the nonlinearity of the Y-function, significant uncertainties arise when extracting G_m and V_T because the accuracy of linear regression depends heavily on the selected V_G range. Consequently, the basic Y-function method exhibited high sensitivity to the chosen V_G range, leading to inconsistencies in the previously reported mobility parameters, as summarized in Table S2. These discrepancies complicated the comparison of the mobility values across different studies and hindered the development of standardized performance benchmarks for 2D FETs. For our BG-FET, when the V_G range was arbitrarily set to 40–50 V for linear regression, the extracted values for G_m, μ_0, θ_1, and V_T were 1.24×10^{-8} A/V, 0.31 $cm^2V^{-1}s^{-1}$, -0.015, and 21.05 V, respectively. Detailed derivations of these values are provided in Supporting Note 1.2.

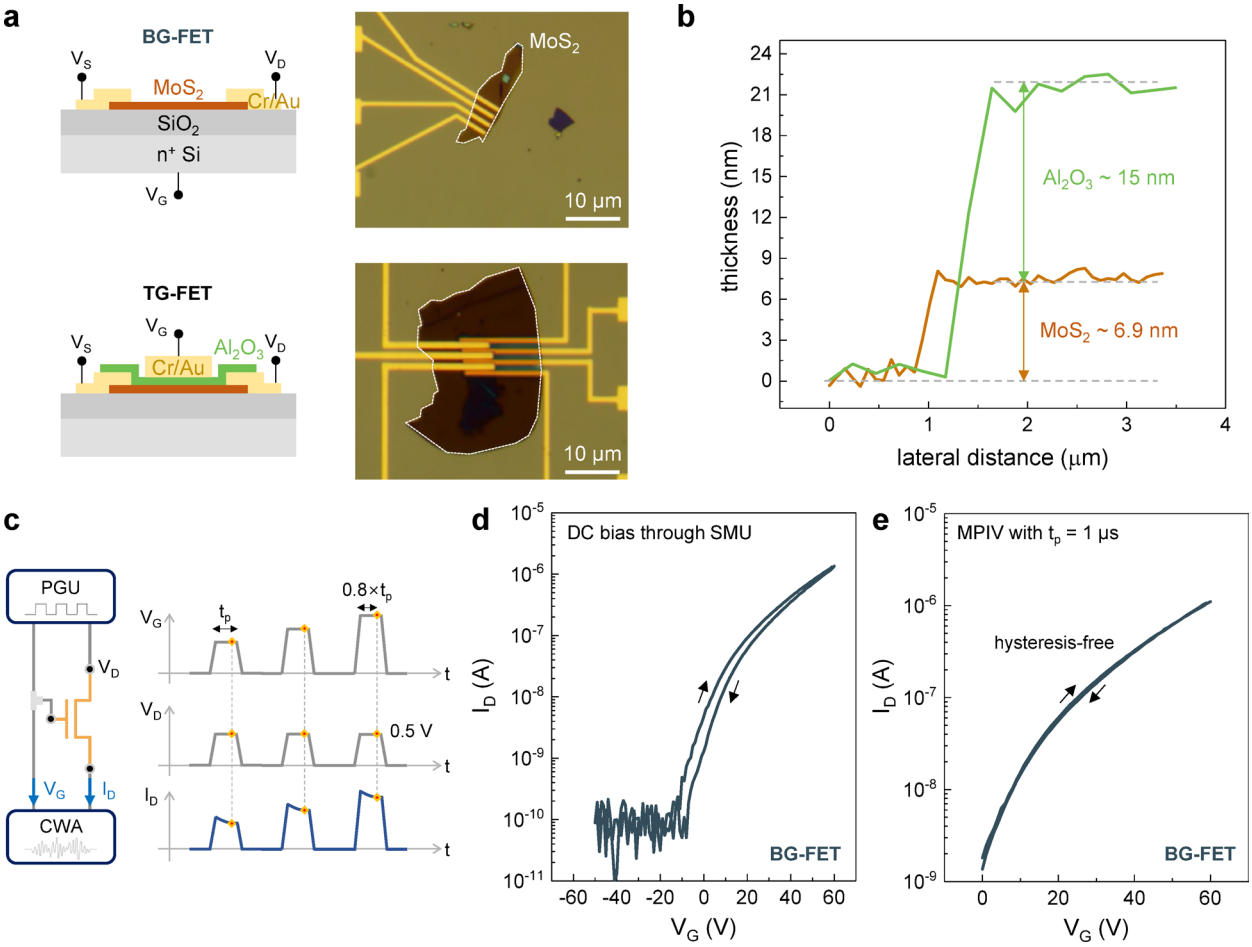


Fig. 1. MoS_2 FETs and measurement setup. (**a**) Schematic representation of BG-FET and TG-FET, along with optical microscope images of the fabricated devices. (**b**) AFM measurements of MoS_2 and Al_2O_3 layer thicknesses. (**c**) Schematic of the measurement setup used for the MPIV method. (**d**) Transfer characteristics of the BG-FET measured using a conventional SMU under vacuum conditions. (**e**) Transfer characteristics of the BG-FET measured using the MPIV method, demonstrating hysteresis suppression and reduced bias stress effects.

Notably, according to Eq. (4), a negative θ_1 implies that the mobility is increased with increasing V_{Gt}. Three potential physical mechanisms may account for this negative θ_1. The first mechanism is the field-induced screening effect. 2D materials, owing to their atomically thin nature, exhibit a charge density that is more directly influenced by the gate field than bulk silicon[22]. As the gate voltage increases, free electrons accumulate in the conduction band, promoting electron–electron interaction. This interaction leads to electric field screening, which can reduce Coulomb scattering at high gate voltages and increase mobility, potentially resulting in a negative θ_1[23]. The second mechanism is the trap-filling effect. The interface trap states between the 2D material and the gate dielectric can significantly influence the carrier mobility[24]. At low gate voltages, these traps capture free electrons and reduce their mobility. However, as the gate voltage increases, these traps become filled, decreasing scattering and enhancing mobility, which can contribute to a negative θ_1[25]. The third potential mechanism is comprised of band-structure modifications. As the gate field increases, the band structure of the 2D material may undergo changes such as band bending. This effect can lower the conduction band minimum and reduce the effective mass of charge carriers, leading to enhanced mobility[26]. Thus, it can be succinctly summarized that the interplay of field-induced screening, trap-filling effects, and band structure modifications underlies the negative θ_1 observed in the BG-FET.

To validate the extracted parameters, we substituted them into the drain current model (Eq. (5)) to simulate the transfer characteristics and calculated the coefficient of determination (R^2 to assess the agreement between the measured and simulated data. Figure 2b plots the measured and simulated I_D and g_m characteristics based on the parameters extracted using the basic Y-function method. For V_G values above V_T, the simulated I_D characteristics closely matched the measured data, with an R^2 value of 0.9990. However, the simulated g_m exhibited a notable discrepancy from the measured data, resulting in a lower R^2 value of 0.9626. This deviation suggests that the basic Y-function method does not accurately capture the mobility parameters.

Next, we employed the polynomial Y-function method, which is detailed in Supporting Note 1.5, to extract these mobility parameters. It begins with a more complex drain-current model expressed as

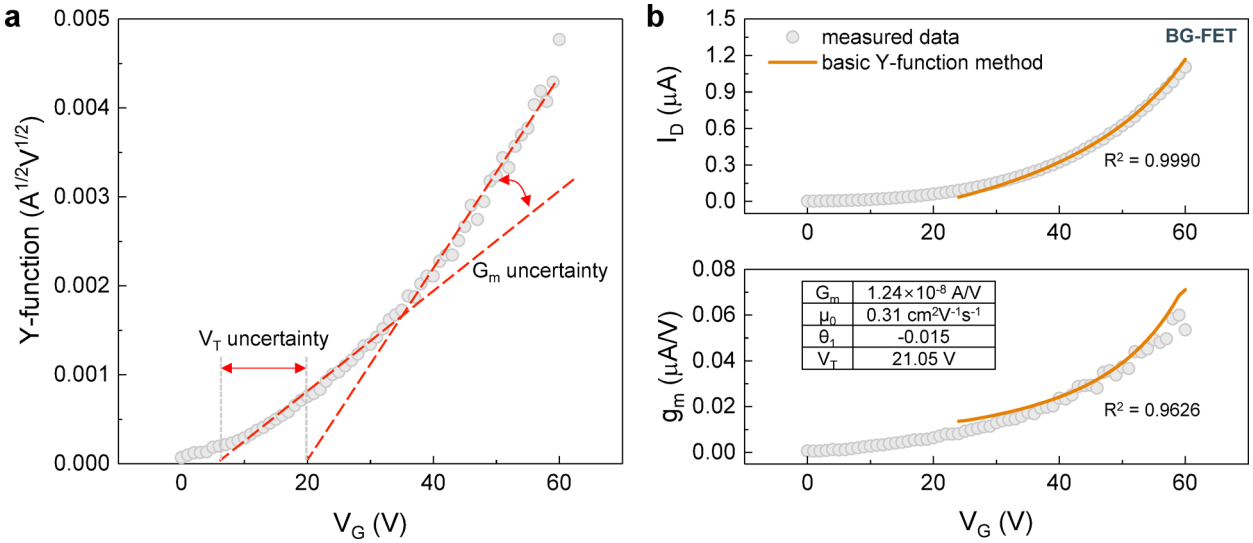


Fig. 2. Limitations of the basic Y-function method. (**a**) Use of the basic Y-function to calculate the V_G of the BG-FET. The extracted parameters exhibit strong dependence on the chosen V_G range, leading to inaccuracies. (**b**) Simulated and measured I_D and g_m characteristics based on parameters extracted using the basic method. The simulated g_m deviates significantly from experimental data, highlighting the inability of this method to account for mobility degradation effects.

$$I_D = G_m \frac{V_{Gt}}{1 + \Theta_1 V_{Gt} + \Theta_2 {V_{Gt}}^2} \tag{6}$$

$$\Theta_1 = \frac{\theta_1 - 2\theta_2 \Delta V_T}{1 + \theta_2 \Delta {V_T}^2}, \ \Theta_2 = \frac{\theta_2}{1 + \theta_2 \Delta {V_T}^2} \tag{7}$$

The polynomial method leverages a recursive algorithm, in which the parameters are iteratively refined until convergence, thereby reducing the sensitivity to the selected V_G range and ensuring a more consistent extraction of the mobility parameters. The recursive process begins with an initial estimate V_T^*, which differs from actual V_T by an error, $\varepsilon = V_T^* - V_T$. A new function $\xi = 1/Y^2$ is defined, which becomes a polynomial function of $1/V_{Gt}^*$ (Equation (S27)). At each iteration step *i*, a polynomial regression is performed on ξ in terms of $1/V_{Gt}^*$, yielding an updated error term ε_i. The threshold voltage estimate is subsequently refined as $V_{T,i+1}^* = V_{T,i}^* - \varepsilon_i$. This iterative refinement continues until $V_{T,i}^*$ converges, yielding a precisely determined V_T and, consequently, the mobility parameters.

Figure 3a illustrates the evolution of $V_{T,i}$ over five iterations, beginning with an initial estimate of $V_{T,0}^*$ = 21.05 V, obtained via the basic Y-function method. Convergence was achieved with a minimal error after five iterations, yielding a final V_T of 11.32 V, which differed significantly from the results of the basic method. Subsequent extraction steps detailed in Supporting Note 1.5 yielded the refined mobility parameters: G_m = 4.38×10^{-8} A/V, $\mu_0 = 0.11$ $cm^2V^{-1}s^{-1}$, $\theta_1 = -0.022$, $\theta_2 = 0.000253$, and $\Delta V_T = 0$ V. Notably, the values of θ_2 and ΔV_T are remarkably small, indicating that the BG-FET, which features a thick 300 nm gate dielectric, does not generate a strong transverse electric field. Consequently, mobility degradation due to field-enhanced interface-related scattering was minimal. Unlike the basic method, the polynomial method accurately extracted θ_2, enabling precise identification of the mechanisms contributing to mobility degradation. To further validate these extracted parameters, they were substituted into the drain-current model (Eq. (6)) to simulate the I_D and g_m characteristics. The resulting simulations closely matched the measured data, as shown in Fig. 3b, with R^2 values of 0.9997 and 0.9899, respectively, surpassing the accuracy achieved using the basic method. Thus, the polynomial Y-function method enables a significantly more accurate extraction of the mobility parameters than the basic method.

Mobility parameters in TG-FET

Finally, we applied both the basic and polynomial Y-function methods to extract the mobility parameters of the TG-FET, following the procedure outlined in Sect. Mobility parameters in BG-FET. Figure 4a presents the results obtained using the basic method. When the extracted parameters were used to simulate the I_D and g_m characteristics, a significant discrepancy was observed between the simulated and measured data. This deviation was caused by the inherent limitations of the basic method, which does not account for additional scattering mechanisms in the TG-FET, such as field-enhanced interface-related scattering. In particular, the g_m characteristics exhibited poor agreement, with an R^2 value of only 0.5835. This result indicates that the basic Y-function method, which relies solely on θ_1, fails to accurately capture the peak behavior of g_m. Consequently, the omission of the key scattering effects leads to an inadequate representation of the actual device behavior.

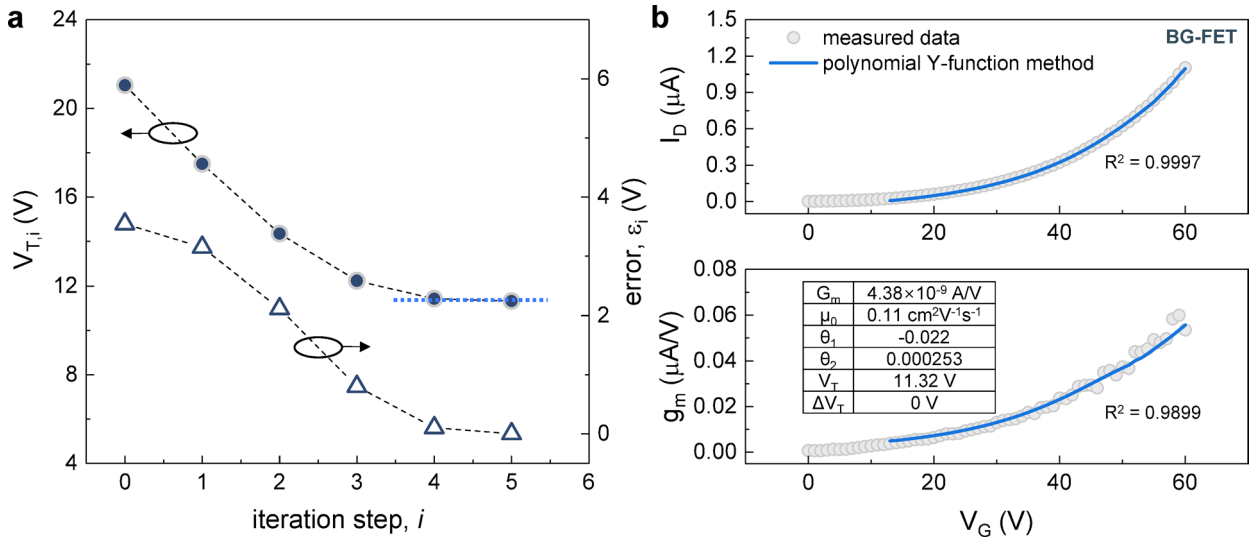


Fig. 3. Advantages of the polynomial Y-function method. (**a**) Iterative refinement of V_T estimation using the polynomial Y-function method. The convergence process significantly reduces extraction uncertainty, enabling more accurate extraction of V_T and other mobility parameters. (**b**) Simulated and measured I_D and g_m characteristics based on parameters extracted using the polynomial method. The close agreement between simulated and experimental data demonstrates the superior accuracy of the polynomial method compared to the basic method.

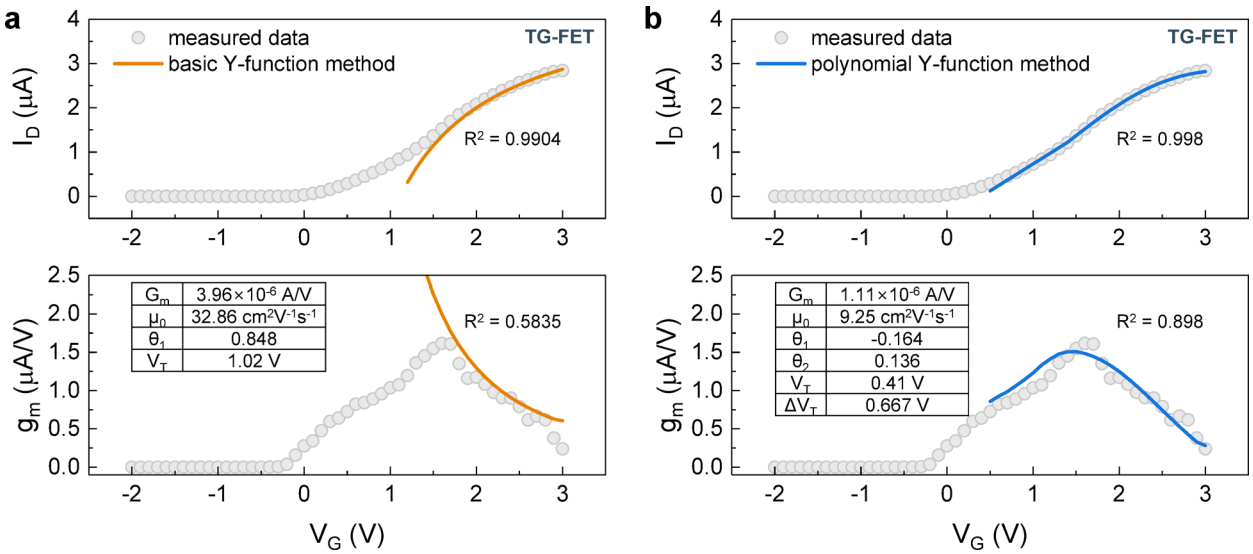


Fig. 4. Comparison of mobility extraction methods in TG-FET. (**a**) Simulated and measured I_D and g_m characteristics obtained using the basic Y-function method. The basic approach fails to capture the g_m peak behavior, resulting in a poor coefficient of determination ($R^2 = 0.5835$). (**b**) Simulated and measured I_D and g_m characteristics using the polynomial Y-function method. The polynomial approach accurately reproduces both I_D and g_m characteristics, revealing the influence of field-enhanced interface-related scattering in the 15 nm Al_2O_3 gate dielectric.

In contrast, Fig. 4b presents the results obtained using the polynomial Y-function method, which accurately reproduced both the I_D and gm characteristics with high precision. Notably, compared to the BG-FET (Fig. 3b), the TG-FET exhibits significantly larger extracted values of θ_2 and ΔV_T. These increases are attributed to the thinner 15 nm Al_2O_3 gate insulator in the TG-FET, which induces a stronger transverse electric field. The intensified field-enhanced interface-related scattering processe, leading to a more pronounced mobility degradation, as reflected in the increased values of θ_2 and ΔV_T. A direct comparison of the extracted mobility parameters between the BG and TG devices reveals distinct differences in transport behavior. Although the TG-FET demonstrates a higher μ_0 compared to the BG-FET, it also exhibits substantially greater field-

enhanced interface-related scattering, as indicated by the increased θ_2 and ΔV_T. This suggests that, while the TG configuration initially benefits from improved channel electrostatics due to the thin top-gate dielectric, it suffers from enhanced surface scattering at higher gate fields. Consequently, carrier transport in the TG-FET undergoes more severe mobility degradation in the On-state region, underscoring the critical role of dielectric engineering in optimizing 2D FET performance. This detailed decomposition of mobility degradation mechanisms has not been fully addressed in previous studies, highlighting the unique capability of the polynomial method to capture these effects with greater accuracy. By enabling a more comprehensive analysis of the scattering mechanisms influencing mobility, the polynomial Y-function method represents a significant advancement over conventional approaches and offers deeper insights into the physical properties that govern 2D FET performance.

Conclusion

This study presents an advanced polynomial Y-function methodology for accurately extracting mobility parameters in 2D FETs, addressing key limitations of conventional approaches. Through a systematic analysis of MoS_2 FETs with both BG and TG configurations, we demonstrated that the proposed method enables precise identification of threshold voltages and mobility degradation factors, including field-enhanced interface-related scattering and Coulombic interactions. Furthermore, this methodology can be extended to other 2D materials such as WSe_2, WS_2, and $MoTe_2$, broadening its applicability and reinforcing its generalizability in the study of 2D FETs. These findings highlight the significant influence of dielectric thickness on carrier mobility, with TG-FETs exhibiting enhanced scattering due to stronger transverse electric fields. The polynomial Y-function approach establishes a refined analytical framework that minimizes extraction uncertainties and provides deeper insight into the physical mechanisms governing charge transport in 2D FETs. In addition to improving extraction precision and mitigating series resistance effects, the method offers a standardized benchmark for mobility characterization, ensuring more reliable and consistent performance evaluations across diverse device architectures. However, it should be noted that the applicability of the polynomial Y-function method to ultra-scaled or near-ballistic 2D FETs remains an open question. In such cases, additional quantum corrections or alternative transport models may be required to maintain extraction accuracy, as discussed in Supporting Note 1.6.

Future research should extend this methodology to other TMD materials to further investigate their distinct mobility degradation mechanisms. In parallel, exploring advanced gate dielectric engineering strategies, such as high-k dielectrics and multilayer dielectric stacks, could enhance 2D FET performance toward realizing high-speed and low-power nanoelectronic applications. Furthermore, while the proposed polynomial Y-function method is applicable to both monolayer and multilayer MoS_2 FETs within the drift-diffusion transport framework, additional physical effects—such as enhanced Coulomb scattering and quantum confinement—may become significant in monolayer devices, particularly at low gate biases. Future studies could refine the methodology by explicitly incorporating these effects, thereby extending its applicability to a broader range of ultra-scaled or quantum-confined 2D FETs.

In addition, it should be emphasized that the extracted mobility parameters (μ_0, θ_1, and θ_2) inherently depend on the intrinsic properties of the specific 2D material being investigated. For instance, the low-field mobility μ_0 is fundamentally determined by the carrier effective mass and the strength of intrinsic phonon scattering, both of which differ among various transition metal dichalcogenides (TMDs) such as WSe_2 and $MoTe_2$. Likewise, the attenuation factor θ_1 mainly reflects phonon-limited scattering and residual Coulomb interactions, which are influenced by the characteristic phonon modes and dielectric screening capability of the material. The θ_2 parameter, which describes additional mobility degradation under higher transverse electric fields, can be significantly affected by the dielectric interface quality, chemical stability of the TMD, and the type of gate insulator or encapsulation used. Therefore, while the polynomial Y-function method provides a generalized framework for mobility extraction in 2D FETs, the absolute values and relative significance of these parameters should always be interpreted in the context of each TMD's unique electronic structure, phonon characteristics, and interface conditions. Benchmarking the extracted results against well-established theoretical and experimental data for each material is essential to ensure reliable mobility characterization when applying this approach to other emerging 2D semiconductors.

Methods

Fabrication of BG-FET The BG-FET was fabricated on a heavily n-doped Si wafer (resistivity < 0.005 Ω·cm), which served as the BG electrode. A 300 nm-thick silicon dioxide (SiO_2) layer was grown on the Si wafer via thermal oxidation. Thin MoS_2 flakes were mechanically exfoliated from bulk MoS_2 (HQ Graphene) using the Scotch tape method and subsequently transferred onto the Si/SiO_2 substrate via a dry transfer technique using a polydimethylsiloxane (PDMS) stamp. The source and drain electrodes were then patterned using electron-beam lithography, followed by the deposition of Cr/Au (10 nm/50 nm) via thermal evaporation. The lift-off process was performed by immersing the devices in acetone and methanol (CH_3OH) for 3–4 h to remove the resist and finalize the electrode patterning.

Fabrication of TG-FET Following BG-FET fabrication, a 15-nm-thick aluminum oxide (Al_2O_3) film, which is a gate dielectric layer, was grown via atomic layer deposition (Nano-ALD2000, IPS) at 350 °C. Electron beam lithography was then performed to define the top-gate electrode region on the Al_2O_3 layer, followed by the deposition of Cr/Au (10 nm/100 nm) via thermal evaporation. A second liftoff process was conducted to complete the TG-FET fabrication.

Data availability

The datasets generated and/or analyzed during the current study are available from the corresponding author on reasonable request.

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Author contributions

J.J., Y.J.L., and H.R. contributed to methodology, validation, and investigation. S.K. supervised the project and was responsible for writing—review and editing. All authors reviewed the manuscript.

Declarations

Competing interests

The authors declare no competing interests.

Additional information

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