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Analysis on performances of ultra-thin vertical MOSFET depending on position of gate–drain misalignment

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In advanced MOSFET design, a vertical-channel structure provides the advantages of a smaller footprint of the transistor cell and stronger immunity against short-channel effects by introducing higher freedom in determining the channel length. For these reasons, vertical devices are still predicted to be an upcoming solution in the most recent technology roadmap. However, due to the cell-to-cell or wafer-to-wafer processing deviation that inevitably exists, it can be quite challenging to locate the gate edges at the exact positions that maximize the device performance. In this work, a series of technology computer-aided design (TCAD) device simulations have been carried out to investigate the effects of gate underlap and overlap structures on the device performance of vertical-channel MOSFETs. The device characterizations were conducted from the aspects of both DC and HF operations for higher completeness of this work, since both are not usually optimized at the same time under the same structural and processing conditions. Under the underlap condition, slight degradation in the on-state current (I_{on}) drivability was observed. On the other hand, a noticeable off-state current (I_{off}) increase was witnessed under the underlap conduction. It is explicitly demonstrated that excessive gate underlap results in non-ideal effects, including degradation of the subthreshold swing (S), worsening of drain-induced barrier lowering, and lowering of the maximum transconductance ($g_{m,Max}$). In the HF analyses, although f_T and f_{max} remained high under overlap and gate–drain alignment conditions, it was observed that both were likely to deteriorate under underlap conditions. As a result, a processing margin in the anisotropic etching of the gate can be obtained for the optimization of the DC and HF performance of vertical-channel MOSFETs, paving the way for a wide variety of low-power and high-speed analog and digital applications. © 2024 The Author(s). Published on behalf of The Japan Society of Applied Physics by IOP Publishing Ltd

1. Introduction

As MOSFETs are aggressively scaled to the extreme, with an effective channel length (L_{ch}) of 10 nm and below, severe short-channel effects (SCEs) have become prevalent, threatening the low-power and high-speed operation capabilities. In order to strengthen the gate controllability and overcome the hindrance in realizing the ideal device operations, novel MOSFET structures are being continuously developed, including the double-gate MOSFET, tri-gate MOSFET or FinFET, and the gate-all-around or nanowire MOSFET.[1–11] In the current commercial FinFET, the channel is wrapped by the gate in all directions except in the bottom direction, through which the transistor is grounded to the bulk substrate.[12,13] Using these approaches, high gate controllability and strong operation stability are acquired, and for these reasons, the FinFET will remain the key device technology until 2025 according to the most recent technology roadmap, the International Roadmap for Devices and Systems (IRDS).[14] In order to obtain even higher gate controllability and to make a way out of the non-ideal device characteristics, the advanced device technologies tend to employ extremely thin channels in the MOSFETs. The reports on ultra-thin-body (UTB) technologies date back more than two decades,[15–17] and UT channels are now being used to construct the most recent devices.[18,19] The last piece can be inserted by introducing a vertical-channel structure for the extension of the highly scaled CMOS technology. Various merits of the vertical channel can be observed, such as a higher cell area efficiency, stronger robustness against SCEs, and a larger degree of freedom in determining the channel length.[20–27] Different types of multiple-gate MOSFETs have been reported,[1,28,29] and the vertical-channel structure is actually found in one of these cases. Compared with the other types, the vertical-channel MOSFET has the smallest footprint and the most ideal current–voltage characteristics.[30] Furthermore, if the device is scaled with a short enough width, a vertical gate-all-around (VGAA) structure is realized. In short, ultra-thin vertical (UTV) technology may have a great deal of universality in advanced MOSFETs. Despite all the advantageous features that can be brought, VGAA and UTV MOSFETs are located at the tail part of the most recent technology roadmap. One of the reasons for this might be the highly complicated integration process. It is usually challenging to achieve vertical alignment between the gate and channel junctions, which is made inevitable by the uncontrollable deviations taking place in the anisotropic dry etching. Deteriorations that might be caused by gate overlap and underlap in the conventional MOSFET devices have been intensively studied.[31–35] In this work, a series of systematic technology computer-aided design (TCAD) device simulations have been conducted to investigate the effects of gate lapping on UTV MOSFET performances (Silvaco ATLAS with 2017 Deckbuild 4.6.2.R interface). The primary performance indicators in DC and HF operations are closely investigated in balance. Finally, the processing margins with deviation tolerance and performance optimization are provided.

2. Device structure and simulation strategies

Figure 1(a) shows a bird's-eye view of the simulated UTV MOSFET structure. The length and thickness of the vertical channel were set to 70 nm and 20 nm, respectively. In addition, the vertical length of the source and drain junctions was 50 nm in all the simulations. The oxide thickness was 1 nm. Since the gate tunneling model was not utilized in this

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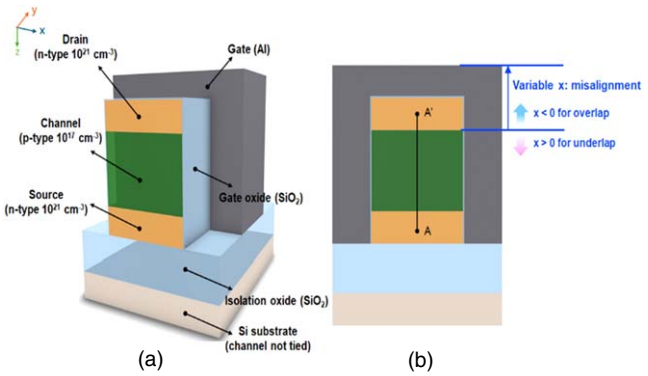


Fig. 1. Device structure of the ultra-thin vertical MOSFET. (a) Aerial view with structure definitions. (b) Cross-sectional view with variable definition.

work, it can be also understood that the effective oxide thickness (EOT) was 1 nm. In the most recent version of IRDS, the EOT is referred to as the capacitive equivalent thickness, and its value is 1 nm. The operating voltage as well as the equivalent oxide thickness were benchmarked from the most recent IRDS (2023 edition) for higher practicability and credibility of the series of device simulations. The source and drain junctions were assumed to have an *n*-type doping concentration of $10^{21}\,\mathrm{cm}^{-3}$ (degenerately doped), and the *p*-type channel doping concentration was $10^{17}\,\mathrm{cm}^{-3}$. A metal gate of Al was employed. The source and drain junctions were positioned at the top and bottom of the vertical channel, respectively. The overall active device region was designed to be isolated from the Si bulk substrate. Figure 1(b) schematically shows a cross-sectional view of the UTV MOSFET, cutting down the channel and the Al gate at the same time. In this figure, it is noteworthy how the overlap and underlap lengths, the independent variables over the following chapters, are quantitatively defined. In order to quantify the misalignment between the gate and drain junction, an independent variable (underlap length) x can be introduced. The metallurgical junction between the channel and drain is the reference location at $x = 0$. If the gate is above this reference line, a gate overlap is formed with a negative value of x, since x is defined as the underlap length. By the same token, if the gate edge is located below the reference line, a gate underlap is formed and the independent variable x has a positive value. The overlap value was varied from $x = -100$ nm up to $x = -20$ nm with four intervals, which represented the cases where the gate was not etched conformally covering the fin, and the gate edge was etched down 20 nm above the reference line. The device performance was also examined under the alignment condition ($x = 0$), in which the gate edge was located at the reference line (channel–drain metallurgical junction) for comparison. Then, the device characteristics were observed under the underlap conditions, varying the underlap length from $x = 20$ nm up to an excessively etched length of $x = 50$ nm. The driving voltage (V_{DD}) was set to 0.65 V as the predicted target value in the year 2025 by the IRDS,[14] rather than to an arbitrarily decided value. For higher credibility and accuracy in the TCAD device simulation results, multiple models were activated simultaneously, including Lombardi's concentration-field-temperature-dependent mobility model, the Shockley–Read–Hall recombination model, the quantum mechanical model with more realistic carrier distributions, and the band-to-band tunneling model with corrections by non-local calculation. The various models above were precisely sorted and combined, avoiding unwanted convergence problems in performing the simulations, and consistently preserved in both DC and radio frequency operation analyses. Quantum meshes were additionally woven.

3. Results and discussion

3.1. Analysis of DC characteristics

Figure 2 shows the transfer curves of the UTV MOSFET with different x values at $V_{DS} = 0.65$ V. As the gate overlap gradually turns to underlap, it is observed that the on-state current (I_{on}) decreases, while the off-state current (I_{off}) increases; they move in opposite directions according to the change in x. Figure 3(a) depicts the I_{on} and I_{off} values as a function of the underlap position. Here, I_{on} and I_{off} are defined as the drain current (I_D) at $V_{GS} = 0.65$ V and 0 V, respectively. Although a strict definition of I_{off} comes with a condition of $V_{GS} = V_{DS} = 0$ V, (V_{GS}, V_{DS}) = (0 V, 0.65 V) referred as standby condition in a stricter sense is defined as the off-state in this work to make it a single-variable (V_{GS}) analysis. The overlap condition has little influence on I_{on} and I_{off}. However, both values show a drastic change as a certain degree of underlap is introduced. More quantitatively, $x = 20$ nm can be traced as the altering point, as shown in Fig. 3(a). Figure 3(b) shows the I_{on}/I_{off} current ratio as a function of the underlap position. As shown in Fig. 3(a) where I_{on} shows a relatively small decrease in terms of the exponent power within a decade, and I_{off} demonstrates an increase to a value more than 100 times higher, I_{on}/I_{off} also reveals a sharp drop at $x = 20$ nm. The reason for the lowering of I_{on} is largely attributed to the increase in series resistance constructed between the recession by the underlap between the drain junction and gate edge. However, I_{off} is not simply governed by the increased series resistance but rather increases, which requires further investigation of the underlying reasons. Figures 4(a) and 4(b) show the energy-band diagrams at $V_{GS} = 0$ V and $V_{DS} = 0.65$ V, under non-underlap and underlap conditions, respectively. The energy bands were obtained along the cutline A-A' in the vertical direction, as indicated in Fig. 1(b). The lateral symmetry was

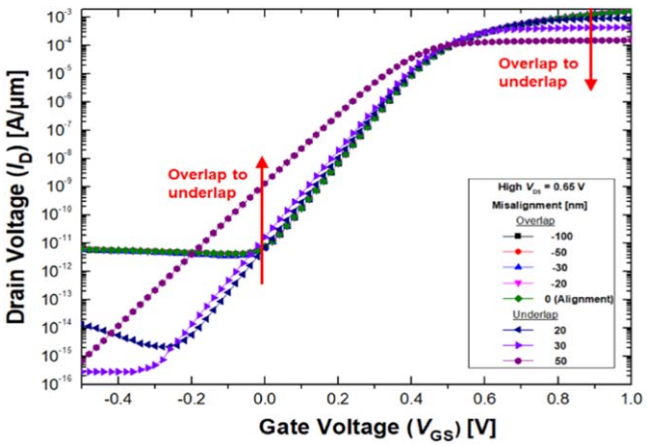


Fig. 2. I_D–V_{GS} curves at different locations of the gate edge (V_{DS} = 0.65 V).

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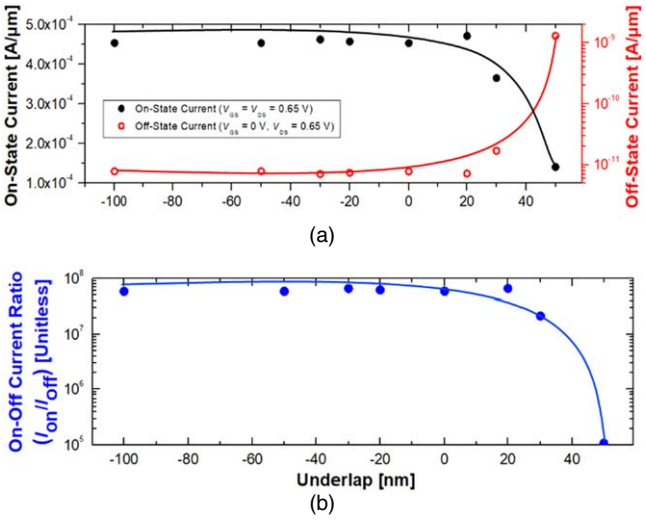


Fig. 3. Current characteristics under different underlap conditions at V_{DS} = 0.65 V. (a) On-state current (I_{on}) and off-state current (I_{off}) as a function of underlap length. (b) I_{on}/I_{off} current ratio as a function of underlap position.

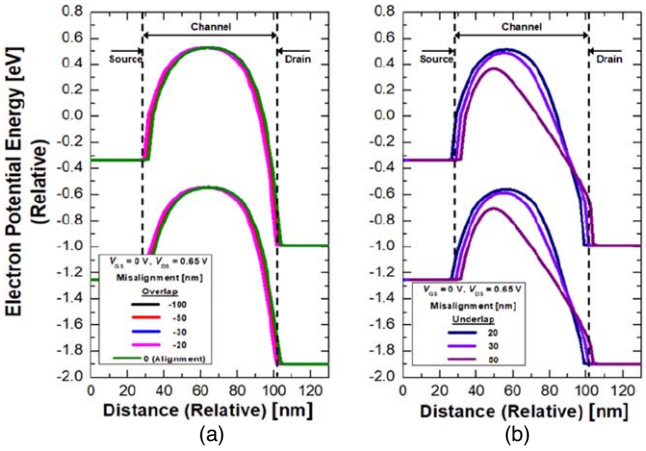


Fig. 4. Energy-band diagrams under off-state bias condition (V_{GS} = 0 V and V_{DS} = 0.65 V). (a) Overlap and alignment conditions. (b) Underlap conditions.

considered by cutting the center. As x is varied from −100 nm (conformal gate wrapping) to 0 nm (gate edge–drain junction aligned), there is little difference among the band structures, as confirmed by Fig. 4(a). On the contrary, Fig. 4(b) reveals that as the underlap misalignment increases, the band structures by underlap positions show marked changes. The Si channel region under the gate shows a parabolic change as a function of position according to the theory on the *pn* junction.[36] However, a larger portion of the Si channel is exposed out of the gate coverage as the underlap becomes severe, and the depletion region between the gate and the drain junction end shows a linear decrease in the band towards the drain junction. This accompanies the lowering of the energy barrier between the source junction and the channel, which leads to a larger injection of source electrons, or equivalently, an increased I_{off}. At the same time, it is shown that the local maximum in the electron potential energy is shifted leftward as the underlap length is increased and the physical gate length is shortened. As a result, the intervening depletion region becomes wider, and the leveling of the electric field across the depletion region becomes more

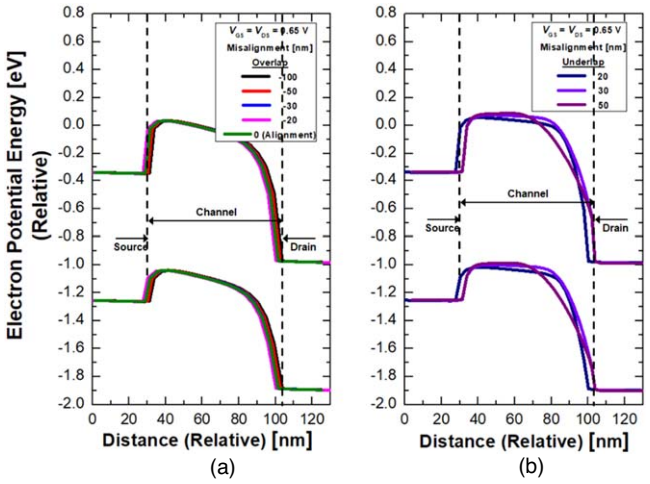


Fig. 5. Energy-band diagrams under on-state bias condition (V_{GS} = V_{DS} = 0.65 V). (a) Overlap and alignment conditions. (b) Underlap conditions.

prominent. Figure 5 demonstrates the distributions of electric fields extracted from the cutline A-A' in Fig. 1(b) across the channel under different underlap conditions. Under overlap conditions, the field distributions are indistinguishable. However, as the underlap edge approaches the source side, the electric field tends to show more drastic distortion and the break-in location of the field increase moves in the source direction.

As a consequence, the electric field is more widely distributed along the depletion region. In relation to Fig. 4(b), the linear band bending and the wider distribution of the electric field at the channel center are closely correlated. It can be reminded that in the actual device fabrication, the underlap position is determined by the anisotropic dry etch of the gate controlled in a timed manner. In order to completely remove a targeted amount of material, over-etching to some degree is performed in most cases. It is proven that the overlap and alignment conditions do not practically threaten the DC characteristics of the UTV MOSFET device, and a certain degree of underlap can be permitted. However, one must expect excessive dry etching to keep the invariance in DC performance. Under the overlap condition, there is little change in the electron potential energy depending on the overlap length once the channel is completely controlled by the gate, as shown in Fig. 5(a). On the other hand, as the underlap length is increased, the location at which the potential energy drop begins moves away from the drain edge, as confirmed by Fig. 5(b). The majority of the potential drop is found between the gate edge and drain junction. Almost the same voltage drop takes place over a wider underlap region and the effective electric field gets smaller, which causes the degradation in I_{on} in Fig. 3(a). The speed of decrease in I_{on} is much larger than that of increase in I_{off} so that I_{on}/I_{off} ratio a rapid roll-off as shown in Fig. 3(b). As the underlap condition becomes severe, the effective potential energy barrier seen by the source electrons toward the channel is lowered, since a larger underlap shortens the effective channel length. Another strong reason can be found in Fig. 6. Under the overlap and alignment condition, the off-state field is effectively concentrated near the drain end. However, as the underlap condition becomes deeper, the electric field shows a wide spatial distribution

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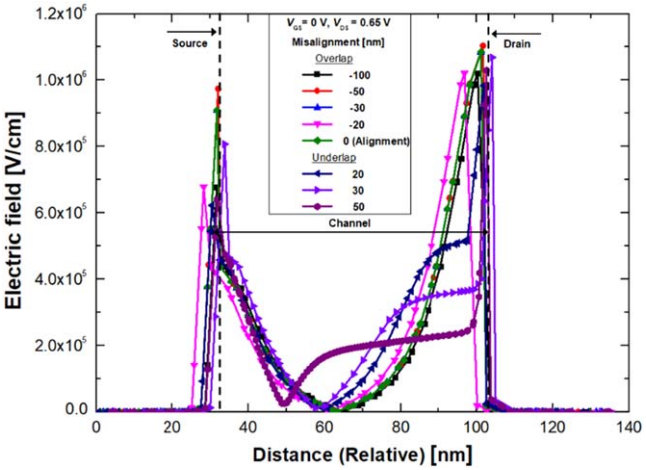


Fig. 6. Electric field distribution in the off-state ($V_{GS} = 0$ V, $V_{DS} = 0.65$ V).

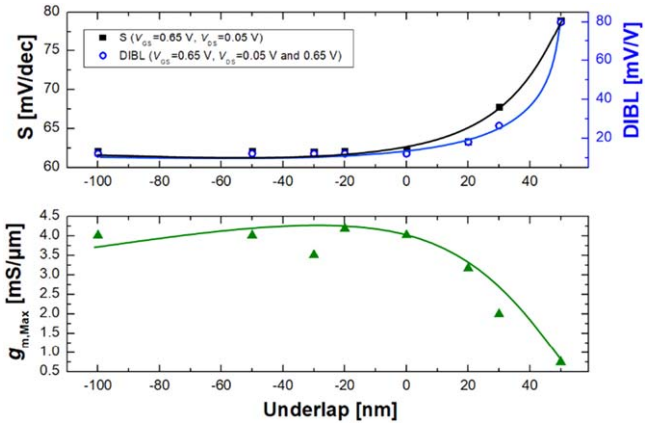


Fig. 8. Fundamental parameters of high-frequency operations. Subthreshold swing (S), DIBL (upper), and $g_{m,Max}$ (lower).

over the underlap region. The highest electric fields are only observed at the drain end, so that I_{off} is effectively suppressed, which is a merit that can be expected by introducing the underlap structure. Figure 7 depicts the distribution of the electron concentration under the off-state condition. As can be confirmed by Fig. 7, the electron concentration increases as the underlap position x gets more positive. This result is also correlated with the lowering of the energy barrier seen by the source electrons, which becomes more distinct, as shown in Fig. 4(b).

3.2. Analysis of high-frequency characteristics

For supplementing the optimal device design with regard to DC performances, HF operation characteristics should be investigated in parallel, in the sense that there is practically no exception in using a highly scaled MOSFET under the HF circumstances no matter which might be the application in between analog and digital integrated circuits. In this regard, it is crucial to further investigate the effects of gate lapping on the HF operation characteristics of the UTV MOSFET. Figure 8 shows the subthreshold swing (S), drain-induced barrier lowering (DIBL), and maximum transconductance ($g_{m,Max}$) as a function of the underlap position. The S values were extracted at a low drain voltage, $V_{DS} = 0.05$ V, in order not to cause a significant deformation in the mathematical induction of S derived from a long-channel device relatively free from SCEs.[37] Under all the simulated overlap conditions, alignment condition, and underlap condition with $x = 20$ nm, the S value was plausibly maintained to be a small value of around 62 mV/dec. However, when excessive etching over 20 nm is carried out, the swing characteristic is rapidly degraded over a small amount of underlap from the critical point, and S reaches 80 mV/dec even under the low V_{DS} condition. S is one of the representative DC parameters of a MOSFET, indicating how large the gate controllability is expected to be. However, at the same time, S can be an indicator of HF performance, since it depends on the depletion capacitance connected to the gate oxide in series.[37] This parasitic capacitor affects the HF operation capability of a MOSFET, so a larger S is not desirable for either DC or HF operations. DIBL shows almost the same tendency with the change in S value. The DIBL values were calculated as the difference between the threshold voltages (V_{th}) divided by that between the high and low V_{DS} values, 0.65 V and 0.05 V. Here, V_{th} was extracted as the V_{GS} at $I_D = 10^{-7}$ A using a constant-current method. Under the overlap condition and the short-range underlap condition ($x < 20$ nm), DIBL is suppressed below a small value of 15 mV/V, which reflects the strong gate controllability benefited by the ultra-thin channel common-gate structure. However, a sharp increase is found with underlap conditions of $x > 20$ nm. $g_{m,Max}$ is depicted as a function of the underlap position as shown in the lower part of Fig. 8. Similar to S and DIBL plotted in the upper part, the degradation of $g_{m,Max}$ becomes prominent above the underlap position of $x = 20$ nm. It is explicitly revealed that all these parameters are intimately correlated with the DC parameters and the underlying physics shown in Fig. 2 through Fig. 7. Finally, the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are traced as a function of the underlap position in Fig. 9. f_T and f_{max} are the most succinct and universal indicators verifying the intrinsic speed of a transistor.[38,39] Although there can be irradiating factors, such as the parasitic capacitances unexpectedly constructed in device structuring, in making a positively correlated relation between f_T and f_{max}, they are substantially affected by g_m.[40] Therefore, as can be predicted to a large degree by

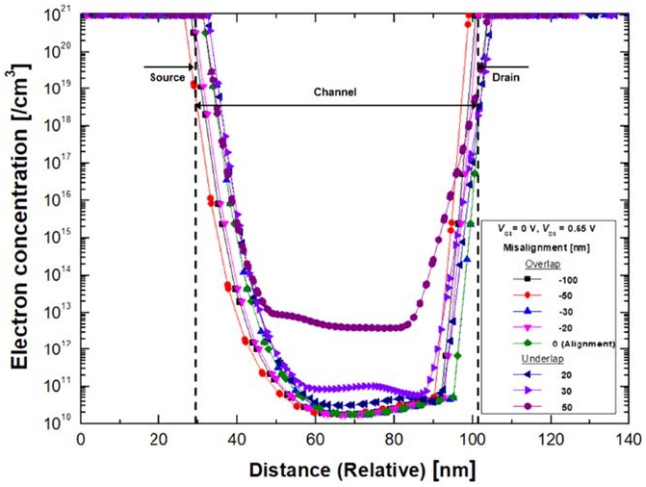


Fig. 7. Distribution of electrons in the channel at $V_{GS} = 0$ V and $V_{DS} = 0.65$ V.

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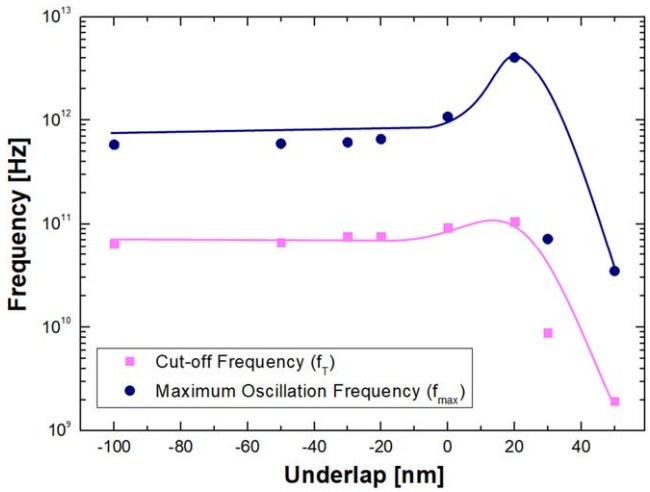


Fig. 9. Cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) as a function of underlap position in drive mode ($V_{GS} = V_{DS} = 0.65$ V).

Fig. 8, f_T and f_{max} show a sudden rolling-off above the underlap position of $x = 20$ nm. As confirmed by Fig. 9, both f_T and f_{max} have local maxima around the alignment condition. The mathematical expressions for f_T and f_{max} of a double-gate transistor can be expressed as the following equations:[41–44)]

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1 + 2(C_{gd}/C_{gs})}} \approx \frac{g_m}{2\pi(C_{gd} + C_{gs})} \approx \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{max} = \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s + R_{ch} + R_g)[g_{ds} + g_m(C_{gd}/C_{gs})]}} \quad (2)$$

where R_s, R_{ch}, and R_g are the source, channel, and gate resistances, respectively. C_{gs}, C_{gd}, and C_{gg} are the gate-to-source, gate-to-drain, and total gate capacitances, respectively. In addition, g_m and g_{ds} are the transconductance and output conductance, respectively. In the MOSFET operation, C_{gd} is reduced when the transistor enters the saturation region, compared with the case when it is in the linear region, which results in an increase in f_T and f_{max} as can be implied by Eqs. (1) and (2). This fundamental relation between C_{gd} and the characteristic frequencies provides a clue to understand the increases in f_T and f_{max} in the negative underlap region (overlap condition). A shorter overlap length leads to a smaller C_{gd}, which results in increases in f_T and f_{max}. However, as the underlap condition becomes more severe, the electrons injected from the source junction are more likely to be confined under the gate region, which gets shorter with the increase in underlap length. Thus, the effective C_{gs} increases, which results in increases in both f_T and f_{max}, as seen in Eqs. (1) and (2). These competing forces between C_{gd} and C_{gs} cause the local maxima in the curves in Fig. 9. Also, although the effective channel length is decreased, the series resistance of the channel increases due to the increase in the underlap length at a fixed metallurgical channel length. This increase in R_{ch} further contributes to the decrease in f_{max}, as can be implied by the relation between f_{max} and R_{ch} in Eq. (2). The increased series resistance and parasitic capacitance induced by the depletion region exposed by excessive dry etching are found to affect the HF performance of UTV MOSFETs. In the device fabrication, a small process variation can significantly impact the overall device performance. The extreme condition in which the gate completely covers the entire channel area, including the drain junction, can be a reference for examining various other cases in this work. Also, at the same time, although they are not in the vertical structures, advanced organic transistors and thin-film transistors are fabricated to have the gate completely covering the drain junction for simplicity in the fabrication process. This work might provide a guideline for the process design not only for the extremely scaled vertical Si devices but also for advanced electron devices in the complete overlap structure.[45,46)] Although the gates on both sides are operated as a common gate in this work, the series of findings can be applied to devices that have either independent gates on both sides or a single common gate overpassing the channel.[47)]

4. Conclusion

In this work, the effects of the overlap and underlap positions on the DC and HF operation characteristics of UTV MOSFETs have been closely investigated. The UTV MOSFET can be thought of as the ultimate structure into which the FinFET can evolve. Furthermore, it has a great deal of expandability to a highly scaled double-gate MOSFET, nanowire FET, etc. Under excessive underlap conditions, a decrease in I_{on} and an increase in I_{off} take place at the same time, which puts the vertical-channel MOSFET away from the ideal logic operations. The excessiveness was quantified to be around 20 nm, presuming a vertical channel length of 70 nm. Although the marginal length can be varied depending on the device structure and the channel length, it has been clearly demonstrated that an excessive underlap harms the performance of the UTV MOSFET. The noteworthy point is that, under the condition of permissibly small underlap, a good device performance provided by the overlap and alignment conditions can still be expected. In this regard, there exists a rather wide margin in determining the effective channel length over the vertical channel, which can be readily reflected in the device fabrication of the UTV MOSFET and relevant novel devices.

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