Pentacene and ZnO hybrid channels for complementary thin-film transistor inverters operating at $2\,\mathrm{V}$

Min Suk Oh, D. K. Hwang, Kimoon Lee, Won Jun Choi, Jae Hoon Kim, and Seongil ImSeungjun Lee

Citation: Journal of Applied Physics **102**, 076104 (2007); doi: 10.1063/1.2785852
View online: http://dx.doi.org/10.1063/1.2785852
View Table of Contents: http://aip.scitation.org/toc/jap/102/7
Published by the American Institute of Physics

Pentacene and ZnO hybrid channels for complementary thin-film transistor inverters operating at 2 V

Min Suk Oh, D. K. Hwang, Kimoon Lee, Won Jun Choi, Jae Hoon Kim, and Seongil Im[a)]
Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea

Seungjun Lee
Information Electronics Engineering, Ewha Womans University, Seoul 120-750, Korea

(Received 4 June 2007; accepted 8 August 2007; published online 3 October 2007)

We report on the fabrication of complementary thin-film transistor (TFT) inverter with organic-inorganic hybrid channels. By adopting organic-pentacene *p* channel and inorganic-ZnO *n* channel, we have fabricated a model device of hybrid complementary TFT inverters at a low channel deposition temperature below 100 °C. Although those *p* and *n* channels were deposited on high-temperature-processed thin gate oxide/*p*-Si here, our complementary device demonstrated good potentials toward air-stable logic applications, operating with an excellent voltage gain of ~26 at 2 V as well as with a dynamic response of ~10 ms. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2785852]

Pentacene thin-film transistors (TFTs) and ZnO-based TFTs have been studied over the last few years as the new representatives of organic TFTs (OTFTs) and inorganic TFTs, respectively, which may replace conventional amorphous-Si TFTs in potential. Since those TFTs could be fabricated at a low process temperature, they are anticipated to open the age of new electronics integrated onto plastic or glass substrates.[1–6] Currently available complementary thin-film transistor (CTFT) inverters are mostly composed of OTFTs for both *p* channel and *n* channel.[7–10] However, the field-effect mobility of *n*-channel OTFTs is generally low (less than 0.1 $cm^2/V\,s$) compared to that of the *p*-channel counterpart (~1 $cm^2/V\,s$), causing substantial difficulties in designing the complementary device,[7–12] and moreover *n*-channel organics are generally known to be more susceptible to atmospheric decay than *p*-channel ones (for example, pentacene is known to be quite stable in air as a *p* channel).[13–16] In order to break through all those difficulties from *n*-channel organics, we recently adopted inorganic *n*-type ZnO on AlO_x dielectric/glass substrate for a new CTFT device because ZnO is known to be an air-stable promising *n*-channel semiconductor with quite a high mobility. As a result, the new CTFT successfully operated although the ZnO channel actually showed much higher field mobility than the organic pentacene which must have been very sensitive to the dielectric surface state.[17] In the present work, the hybrid CTFT with *p*-channel pentacene and *n*-channel ZnO was again investigated as a model device to provide symmetric electron and hole current behavior when fabricated on a highly capacitive thin gate oxide/*p*-Si substrate with smooth surface. Here our CTFT inverters with the organic-inorganic hybrid channels demonstrate an excellent maximum voltage gain of ~26 with a dynamic response of ~10 ms at a low operating voltage of 2 V.

Our CTFT inverters were fabricated on 12.5-nm-thick Al_2O_3/SiO_2 dielectric double layered oxide. The dielectric was composed of a 10-nm-thick atomic-layer-deposited (ALD) (at 450 °C) top Al_2O_3 layer and 2.5-nm-thick high quality thermal SiO_2 on a *p*-Si substrate (obtained from Samsung Electronics Inc.). After dielectric substrate cleaning, 60-nm-thick ZnO channels (area of $500\times500\ \mu m^2$) were deposited through a shadow mask at 100 °C by 100 W rf sputtering of ZnO targets (99.999%) in a vacuum chamber. Then 50-nm-thick pentacene (Aldrich Chem. Co., 99% purity) channels were patterned beside ZnO channels through the same shadow mask (area of $500\times500\ \mu m^2$) by thermal evaporation at room temperature. We fixed the deposition rate to 1 Å/s for thermal evaporation using an effusion cell in a vacuum chamber. Aluminum (Al) and gold (Au) source/drain (*S*/*D*) electrodes were sequentially deposited by thermal evaporation for *n*-type ZnO and *p*-type pentacene channels, respectively; the two metals are known as standard electrodes for ZnO and pentacene. The channel length (*L*) was 90 μm and the width (*W*) was 500 μm. Indium was used as an ohmic-contact electrode for the *p*-Si back gate. After the electrical properties of *n*- and *p*-type TFTs were separately measured, the ZnO and pentacene TFTs were connected by thermally evaporated thin aluminum bar, which is the final process for the fabrication of a CTFT inverter with organic-inorganic hybrid channels. All electrical characteristics of our hybrid CTFTs, unit ZnO TFTs, unit pentacene TFTs, and the quasistatic *C-V* were measured with a semiconductor parameter analyzer (HP4155C, Agilent Technologies) at room temperature in the dark and in an air ambient with the relative humidity of ~45%. The dynamic response of our CTFT device was measured with a function generator (AFG310, Sony/Tektronix) and an oscilloscope (TDS210, Tektronix). The *C-V* measurements at 1 MHz were performed with an *LCR* meter (HP 4284, Agilent Technologies).

Figures 1(a) and 1(b) show a three-dimensional schematic view of our CTFT inverter and a photographic plan view of two inverter sets, respectively. In particular, we examined the interface between organic-pentacene channel and Au and that between inorganic-ZnO channel and Al, magnifying those two channel/electrode borders taken from the

[a)]Author to whom correspondence should be addressed. Tel.: 82-2-2123-2842. FAX: 82-2-392-1592. Electronic mail: semicon@yonsei.ac.kr

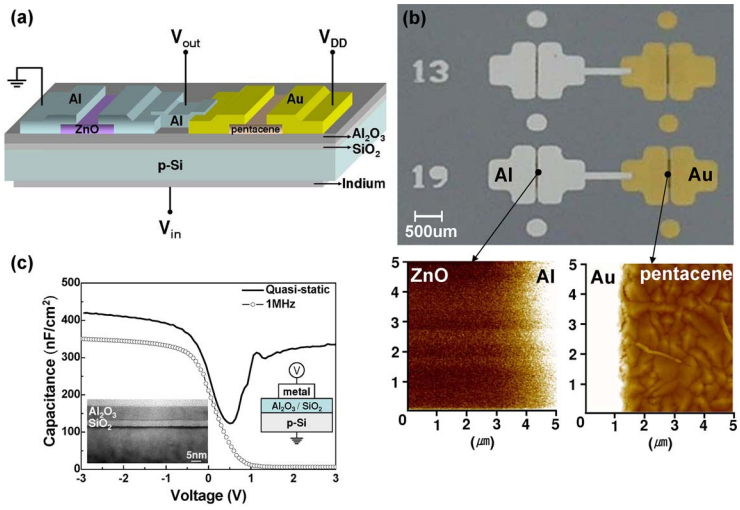

FIG. 1. (Color online) Organic-inorganic hybrid CTFT device schemes and *C-V* characteristics of our dielectric substrate. (a) three-dimensional schematic view of our CTFT inverter. (b) Photographic plan view of two inverter sets and atomic force microscopy (AFM) images of organic-pentacene–Au and inorganic-ZnO–Al borders as taken from the 19th inverter set. (c) Capacitance-voltage (*C-V*) characteristics of our Al_2O_3/SiO_2 gate dielectric film. For the accumulation state, a negative bias was applied on Al or Au electrode.

19th inverter set. Figure 1(b) displays the atomic force microscopy (AFM) images (XE-100, PSIA) of these borders. Due to the geometry of our TFT devices, the surface images for the Al and Au sides appear much brighter than those of pentacene and ZnO, which appear similar to those reported previously.[18,19] The capacitance-voltage (*C-V*) characteristics of our Al_2O_3/SiO_2 gate dielectric film are in Fig. 1(c). For the *C-V* measurement, we used 300-μm-diam Al and Au dots as patterned between the hybrid channel inverters [see Fig. 1(b)]. In the accumulation state (negative bias on the Al or Au electrode) of the *p*-Si substrate, a high capacitance of 350 nF/cm^2 was observed from the 12.5-nm-thin double layer dielectric in a high frequency (1 MHz) *C-V* measurement and the dielectric displayed an inversion of the *p*-Si substrate at less than +1 V under a quasistatic measurement condition, confirming that the dielectric/*p*-Si interface is of high quality. The thickness of the double layer oxide was examined by high-resolution transmission electron microscopy (HRTEM) (JEM 3010, JEOL), as seen in the inset micrograph. The root-mean-square (rms) roughness of our double layer dielectric was less than 0.3 nm.

Figure 2(a) displays the drain current–drain voltage curves (I_D-V_D) obtained from the p-channel pentacene and the *n*-channel ZnO TFT. Under a low gate bias (V_G) of 3 V, quite a high saturation current of more than 2.5 μA was achieved from both devices, with almost full saturation at a drain bias of 3 V. Although the current level of the pentacene TFT appeared slightly higher (~3.5 μA) than that of the ZnO TFT, our hybrid TFT pair was expected to operate well as a complementary device with the same width (*W*) and length (*L*) dimensions for the two channels. Figure 2(b) shows the $\sqrt{I_D}$-V_G curves obtained at a drain bias of 3 V for the ZnO TFT and −3 V for the pentacene TFT. For the pentacene TFT the estimated saturation field-effect mobility is 1.03 $cm^2/V\,s$ and the threshold voltage (V_T) is −0.57 V, while for the ZnO TFT, the saturation field-effect mobility is 1.12 $cm^2/V\,s$ and the threshold voltage (V_T) is 1.05 V. Since the mobilities and threshold voltages of the pentacene and ZnO TFTs are similar, the transfer curves for the two devices appeared almost symmetric while retaining simple device geometry with the same *W*/*L* ratio for the *p* and *n* channels. Each device exhibited a weak hysteresis resulting in a relatively small V_T shift of ~0.15 V for both TFTs. In the case of the pentacene TFT, the relevant hysteresis mechanism has already been reported and it is attributed to certain interfacial electron traps (such as hydroxyl groups, OH–) that initially existed on hydrophilic dielectric oxide surface.[20,21] For the ZnO TFT, some electrons of the ZnO channel may be injected into the very surface of Al_2O_3 during a positive gate bias swing so that the electron-induced (negatively charged) surface causes the positive V_T shift during a reverse swing.[22] Figure 2(c) shows the $\log_{10} I_D$ vs V_G curves for the two TFT devices. The on/off current ratios of the pentacene TFT and

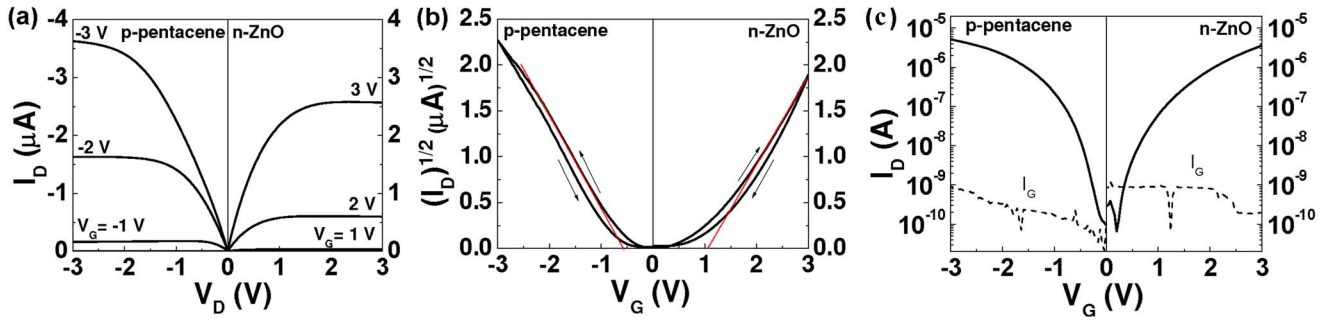

FIG. 2. (Color online) Electrical properties of *p*-channel pentacene TFT and *n*-channel ZnO TFT. (a) Drain current–drain voltage (I_D-V_D) output curves obtained from the *p*-channel pentacene TFT and *n*-channel ZnO TFT. (b) $\sqrt{I_D}$-V_G curves obtained at a drain bias of 3 V for ZnO TFT and −3 V for pentacene TFT. Field-effect mobilities were 1.12 and 1.03 $cm^2/V\,s$ for ZnO and pentacene TFTs, respectively, while V_T were 1.05 and −0.57 V. (c) $\log_{10} I_D$ vs V_G transfer curves for the two TFT devices. S.S. values were 0.11 and 0.17 V/decade for ZnO and pentacene TFTs, respectively, while on/off current ratios were 1.2×10^4 and 2.1×10^4.

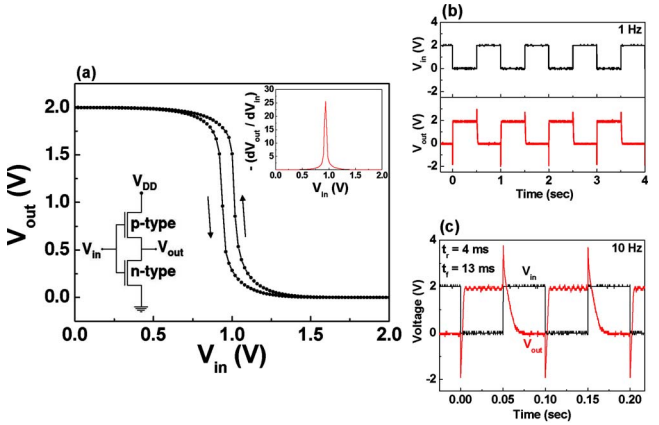

FIG. 3. (Color online) Device performances of our hybrid CTFT inverter. (a) Static behavior of our inverter circuit composed of *p*-channel pentacene TFT and *n*-channel ZnO TFT (left-side inset). It operates well at a low V_{DD} of 2 V with a high gain $(-dV_{out}/dV_{in})$ of ~26 (right-side inset). (b) Dynamic actions of the CTFT inverter at a low frequency (1 Hz) and (c) those at an elevated frequency (10 Hz).

ZnO TFT turn out to be about 10^4 while their subthreshold swings $(S.S.=dV_G/d\log_{10} I_D)$ are 0.17 and 0.11 V/decade, respectively. These S.S. values are good enough for the two channels of our CTFT to operate properly. The maximum gate leakage current (I_G) was less than 1 nA for both TFTs (dotted lines).

Figure 3(a) shows the static behavior of our CTFT inverter with the hybrid channels fully operational at a low supply voltage (V_{DD}) of 2 V although a weak hysteresis of 80 mV is also shown, reflecting the hysteresis of the unit TFT devices. The schematic of the inverter circuit consisting of a pentacene TFT and a ZnO TFT for *p* and *n* channels, respectively, is shown in the left inset. The inverter response to stage switching was clearly observed between 0 and 2 V for both input directions, displaying a high maximum voltage gain $(-dV_{out}/dV_{in})$ of ~26 (see the right inset). The origin of the hysteresis during inverter action is due to that of individual organic TFTs or inorganic TFTs. When the inverter is swept from 0 to 2 V via input voltage, the pentacene channel itself experiences a substantial sweep from −2 to 0 V while the ZnO channel does so from 0 to 2 V. On the other hand, when the inverter is swept from 2 to 0 V, the two TFTs go through the bias sweep in opposite directions. Considering the hysteresis behavior of the two TFTs in Fig. 2(b), we now understand the nature of the hysteresis in our inverter. As a matter of fact, the performances of our CTFT inverter are quite comparable to or surpassing those of previously reported complementary thin-film devices in terms of voltage gain and driving voltage.[7–10] In Figs. 3(b) and 3(c), the dynamic actions of our CTFT inverter are demonstrated. At a low frequency (1 Hz), the inverting action was clearly observed along with the discharging- and charging-induced signal peaks (or *RC* delays at on and off switching). This *RC* time delay was unavoidable because of a large overlap capacitance between V_{in} and V_{out} probes in our simple inverter structure. Measurements at an elevated frequency (10 Hz), carried out to observe the *RC* time delay in detail, show that the rising (t_r) and falling times (t_f) in our inverter are substantially different, about 4 and 13 ms, respectively. This is also understandable if we consider the difference between the on-state current levels of the pentacene and ZnO channels under 2 V gate bias [Fig. 2(a)]. (Channel carriers will discharge the overlap capacitance region and the channel current for pentacene is approximately three times larger than that for ZnO.) These delays can be minimized with more practical designs avoiding the overlap between the source/drain and gate electrodes.

In summary, the essence of our approach is the fact that ZnO can be deposited at a low temperature (<100 °C), serving as a stable *n*-channel semiconductor, with a high field-effect mobility, equivalent to that of pentacene employed as a *p*-channel semiconductor. Based on the high gain and decent dynamic actions of our model device of CTFT inverter, we now conclude that our complementary device technique using organic-pentacene (*p*-type) and inorganic-ZnO (*n*-type) hybrid channels is quite a simple and promising way to realize stable low-voltage low-temperature-processed thin-film electronics.

The authors acknowledge the financial support from KOSEF (Program Nos. M1-0214-00-0228 and R01-2006-000-11277-0) and Brain Korea 21 program. S.I. also thanks K. H. Joo at Samsung Electronics Inc. for supplying the high quality double layer dielectrics. M.S.O. was supported by the Seoul Science Fellowship.

[1] H. Sirringhaus, N. Tessler, and R. H. Friend, Science **280**, 1741 (1998).
[2] C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, Science **283**, 822 (1999).
[3] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schutz, S. Maisch, F. Effenberger, M. Brunnbauer, and F. Stellacci, Nature (London) **431**, 963 (2004).
[4] E. M. C. Fortunato, P. M. C. Barquinha, A. C. M. B. G. Pimentel, A. M. F. Goncalves, A. J. S. Marques, L. M. N. Pereira, and R. F. P. Martins, Adv. Mater. (Weinheim, Ger.) **17**, 590 (2005).
[5] P. F. Carcia, R. S. McLean, and M. H. Reilly, Appl. Phys. Lett. **88**, 123509 (2006).
[6] J. F. Wager, Science **300**, 1245 (2003).
[7] H. Klauk, M. Halik, U. Zschieschang, F. Eder, D. Rohde, G. Schmid, and C. Dehm, IEEE Trans. Electron Devices **52**, 618 (2005).
[8] S. D. Vusser, S. Steudel, K. Myny, J. Genoe, and P. Heremans, Appl. Phys. Lett. **88**, 162116 (2006).
[9] M. H. Yoon, H. Yan, A. Facchetti, and T. J. Marks, J. Am. Chem. Soc. **127**, 10388 (2005).
[10] T. D. Anthopoulos, S. Setayesh, E. C. P. Smits, M. Cölle, B. de Boer, E. Cantatore, P. W. M. Blom, and D. M. de Leeuw, Adv. Mater. (Weinheim, Ger.) **18**, 1900 (2006).
[11] D. J. Gundlach, K. P. Pernstich, G. Wilckens, M. Gruter, S. Haas, and B. Batlogg, J. Appl. Phys. **98**, 064502 (2005).
[12] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, Nature (London) **434**, 194 (2005).
[13] C. D. Dimitrakopoulos and P. R. L. Malenfant, Adv. Mater. (Weinheim, Ger.) **14**, 99 (2002).
[14] C. R. Kagan and P. Andry, *Thin-Film Transistors* (Dekker, New York, 2003), p. 325.
[15] W. J. Kim, W. H. Koo, S. J. Jo, C. S. Kim, H. K. Baik, J. Lee, and S. Im, Electrochem. Solid-State Lett. **8**, G341 (2005).
[16] Ch. Pannemann, T. Diekmann, and U. Hilleringmann, J. Mater. Res. **19**, 1999 (2004).
[17] M. S. Oh, D. K. Hwang, K. Lee, S. Im, and S. Yi, Appl. Phys. Lett. **90**, 173511 (2007).
[18] D. K. Hwang, C. S. Kim, J. M. Choi, K. Lee, J. H. Park, E. Kim, H. K. Baik, J. H. Kim, and S. Im, Adv. Mater. (Weinheim, Ger.) **18**, 2299 (2006).
[19] K. Lee, J. H. Kim, S. Im, C. S. Kim, and H. K. Baik, Appl. Phys. Lett. **89**, 133507 (2006).
[20] D. K. Hwang, K. Lee, J. H. Kim, S. Im, J. H. Park, and E. Kim, Appl. Phys. Lett. **89**, 093507 (2006).
[21] G. Gu, M. G. Kane, J. E. Doty, and A. H. Firester, Appl. Phys. Lett. **87**, 243512 (2005).
[22] R. B. M. Cross and M. M. De Souza, Appl. Phys. Lett. **89**, 263513 (2006).