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Multi-layered nanocomposite dielectrics for high density organic memory devices

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We fabricated organic memory devices with metal-pentacene-insulator-silicon structure which contain double dielectric layers comprising 3D pattern of Au nanoparticles (Au NPs) and block copolymer (PS-b-P2VP). The role of Au NPs is to charge/discharge carriers upon applied voltage, while block copolymer helps to form highly ordered Au NP patterns in the dielectric layer. Double-layered nanocomposite dielectrics enhanced the charge trap density (i.e., trapped charge per unit area) by Au NPs, resulting in increase of the memory window (ΔV_{th}). © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4907320]

Organic memory devices have been of great interests due to their simple structure, light weight, flexibility, and large-area and low-cost processability.[1–5] Nano-floating gate memory is one of the representative organic memory devices which use nanocrystals (e.g., gold nanoparticles; Au NPs) embedded in a transistor dielectric layer as a charge-trapping element.[5–12] In this device, transconductance of semiconductor channel is controlled by stored charge carriers in the nanocrystals via application of external gate field. Charge trapping can be manipulated by metal species, size, and spatial density of the NPs. To this end, there has been extensive research on metal nano-floating gates by adjusting species, size, and distribution of NPs in dielectric layers in order to obtain high performance memory devices.[13–16] Au NPs are typically used as charge trapping sites deposited via sputtering[5] or solution process[15–17] which induced reproducible and reliable threshold voltage (V_{th}) shift both in positive and negative direction depending on the polarity of charge carriers. Spatially distributed large size copper NPs showed very long charge retention time approaching 10 years.[18] Although there has been a remarkable progress in organic memory devices based on metal NPs, it should be further improved to be available in commercial products in terms of memory capacity, retention time, reliability, and low-cost processability.

Here, we report on an organic flash memory element with high memory capacity by using multi-stacked block copolymer (BCP) dielectrics. Block copolymers which contain both hydrophilic and hydrophobic blocks in a chain can simply form specific nanostructures (e.g., sphere, lamellar, or cylindrical morphology) via self-assembly as a function of volume fraction of each block.[17] Using this property, Au NPs can only be localized within one phase of the BCP matrix due to the attractive interaction between the Au NPs and a BCP phase. The size and density of Au NPs can be controlled by varying the volume fraction of each block or the loading ratio of the Au NP precursors.[19] Nanostructured BCP matrix prevents the aggregation of Au NPs in the dielectric, so that it affords a high degree of Au NPs arrangement and induces spatial confinement of trapped charges.[20–22] Furthermore, multi-stacked BCP-based dielectric layers with 3D patterned Au NPs were achieved by employing photo-crosslinking layer between each BCP layers. The vertically

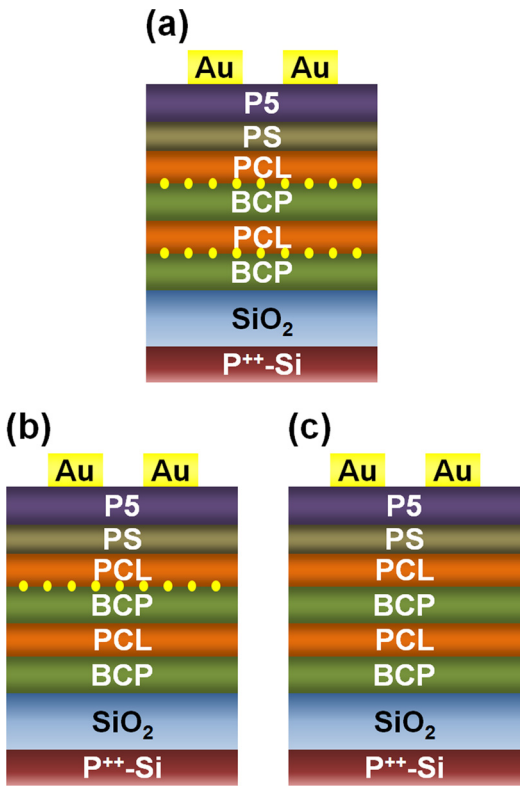

FIG. 1. Schematic of organic memory devices (P5: Pentacene (40 nm), PS: polystyrene (10 nm), PCL: photo-crosslinking layer (10 nm), BCP: block copolymer; PS-b-P2VP (25 nm), SiO_2 (100 nm)), (a) organic memory with double layers of Au NPs (denoted as D-OM), (b) organic memory with single layer of Au NPs (S-OM), (c) without Au NPs (N-OM).

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stacked Au NPs could remarkably increase the number of charge carriers per unit area stored in metallic nano-floating-gates, resulting in large memory window for multi-level memory.[22,23]

Fig. 1 shows a schematic of organic memory devices. The organic memory with double layers of Au NPs (D-OM) was fabricated on a p^{++} Si (for a control gate electrode) wafer with thermally grown 100 nm thick SiO_2 layer (as a charge blocking dielectric). Substrates (2.0 cm × 2.0 cm) were cleaned by bath sonication sequentially in acetone (10 min) and isopropyl alcohol (10 min), followed by O_2 plasma for 1 min. A solution of polystyrene-block-poly-2-vinylpridine (PS-b-P2VP) (0.5 wt. %; PS_{50}-b-$P2VP_{16.5}$, Polymer Source) in toluene was spin-coated onto the substrate at 2000 rpm. Next, the substrate was immersed in aqueous solution of 1:1 $HAuCl_4$/HCl mixture (0.01 M for each) for 20 min to pattern Au salt on the BCP surface. After metal salt deposition, the substrate was washed with DI water to remove loosely bound salts from the BCP surface. Then, the substrate was dipped into freshly prepared aqueous solution of $NaBH_4$ (3.75 mg/mL) for 30 s to reduce $HAuCl_4$ to Au NPs ($HAuCl_4 + 4\ NaBH_4 + 12\ H_2O \rightarrow Au + 4\ B(OH)_3 + 4\ NaCl + 29\ H^+$). Fig. 2(a) shows the scanning electron microscopy (SEM) image of well-patterned Au NPs on the BCP layer. The size and spatial density of the Au NPs were calculated to be around 12 nm and 7.5–8.2 × 10^{10} cm^{-2}, respectively. After forming the first nanocomposite layer, photo-crosslinker (4,4′-diazido-2,2′-stilbene disulfonic acid disodium salt tetrahydrate, Aldrich) in ethanol solution (1 wt. %) was dropped onto the substrate, kept for 3 min, and then spin-coated at 6000 rpm for 30 s. The photo-crosslinking was performed under ultraviolet (UV) light ($\lambda = 254$ nm) irradiation for 10 min. Second BCP layer was formed onto the first layer following the same procedure as described above. The spatial density of Au NPs on the second layer (2.4–4.4 × 10^{10} cm^{-2}, see Fig. 2(b)) was slightly lower than that of the first layer but had a similar NP size. Thereafter, a PS ($M_w = 280\,000$ g/mol, Aldrich) charge tunneling layer was deposited onto the multi-stacked charge storage layers by spin-coating (3 mg/ml in toluene, 5000 rpm) to ensure smooth surface roughness which is favorable for a highly ordered semiconductor deposition as well as to prevent from undesirable trapping of mobile holes at the interface.[23–26] The root-mean-square roughness of the resulting surface was 1.3–2.2 nm. Each layer (BCP, photo-crosslinker, and PS layer) was annealed in vacuum oven at 40 °C for over 12 h. Pentacene layer was deposited by thermal evaporation (40 nm thickness, 0.04 nm/s deposition rate). The Au source/drain electrodes were finally defined by using metal shadow mask with channel length (L) and

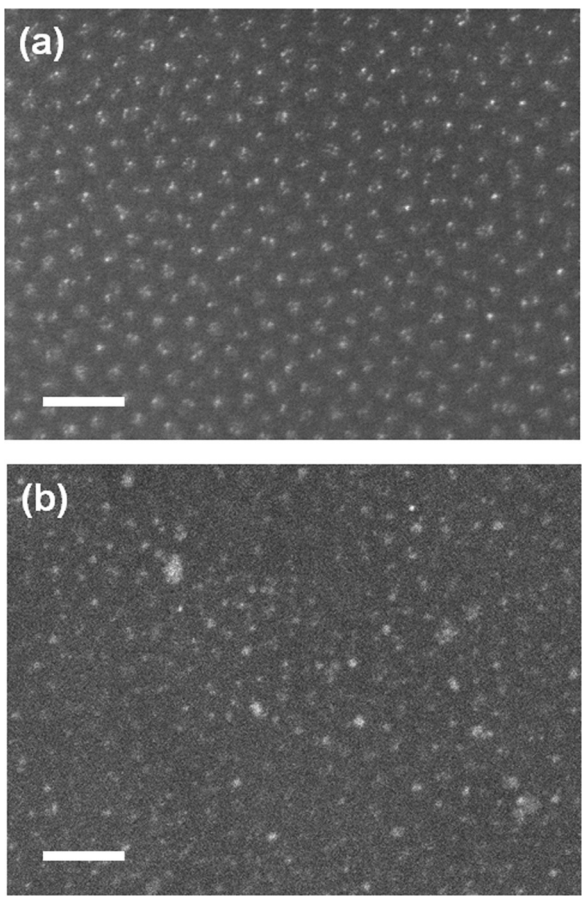

FIG. 2. SEM images of Au NPs on block copolymer layer: (a) first layer of Au NPs, (b) second layer of Au NPs (scale bar, 100 nm).

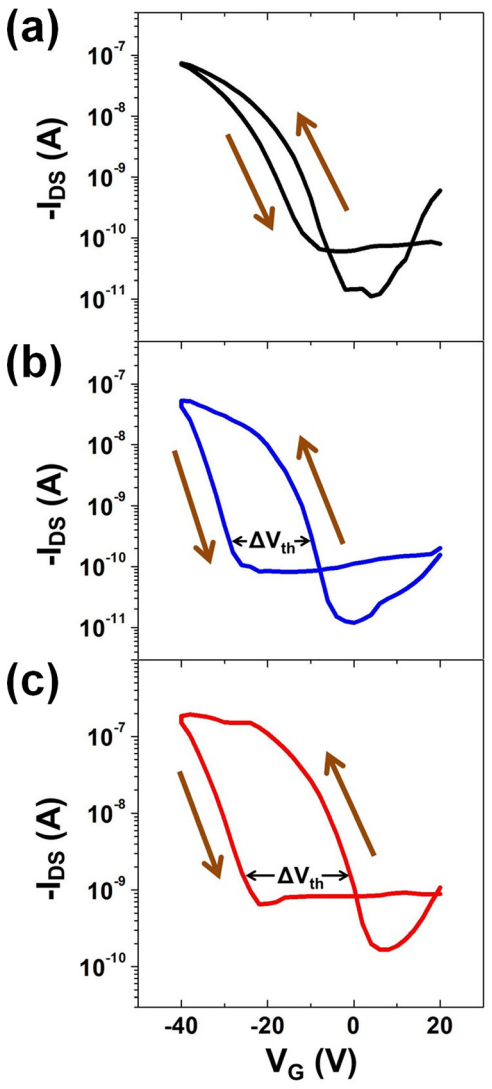

FIG. 3. Transfer characteristics of the organic memory devices as a function of gate voltage at constant $V_{DS} = -60$ V: (a) N-OM, (b) S-OM, and (c) D-OM.

TABLE I. Measured fundamental characteristics of organic memory devices: field-effect mobility (μ), initial threshold voltage (V_{th}), V_{th} shift (ΔV_{th}), current on/off ratio (I_{on}/I_{off}), total stored charge per unit area, and the number of trapped charge carriers per Au nanoparticle.

	μ ($cm^2\ V^{-1}\ s^{-1}$)	Initial V_{th} (V)[a]	ΔV_{th} (V)	I_{on}/I_{off}	Total trapped charge per unit area (C/cm^2)	Number of trapped charge per Au nanoparticle
N-OM	0.0005	−4.51	~3.32	6.7×10^3	6.01×10^{-8}	…
S-OM	0.0003	−8.13	~19.1	5.7×10^3	3.63×10^{-7}	51.6–94.6
D-OM	0.0003	6.14	~30.3	2.0×10^3	5.82×10^{-7}	28.8–36.7

[a]defined as the threshold voltage for the forward (initial) scan of the gate voltage.

width (W) of 100 and 2000 μm, respectively. The memory device characteristics were measured using Keithley 4200-SCS in ambient air.

Fig. 3 shows the transfer characteristics (drain current I_{DS} vs gate voltage V_G) of organic memory devices with various dielectrics; (*i*) double layers of Au NPs (denoted as D-OM), (*ii*) a single layer of Au NPs (S-OM), and (*iii*) without Au NPs (N-OM), and obtained device parameters are summarized in Table I. The charge storage properties of the Au NPs were verified via dual sweeps of V_G from +20 to −40 V and reversed from −40 V to +20 V at a gate voltage sweep rate of 2 V/s with constant drain voltage (V_{DS}) of −60 V. By application of high negative gate bias, holes from pentacene active channel can transfer through the thin tunneling layer and be trapped at the Au NPs in the dielectrics. As shown in Fig. 3(a), N-OM device exhibited little hysteresis. On the other hand, S-OM and D-OM showed significant counter-clockwise hysteresis with a memory window (defined as the maximum difference of the threshold voltage shift (ΔV_{th}) in the bi-directional V_G sweeps) of 19.1 V and 30.3 V, respectively (see Figs. 3(b) and 3(c)). From the values of memory windows, the amount of stored charges (Q_t) in the dielectric was calculated by employing the equation

$$Q_t = C_i \times \Delta V_{th},$$

where C_i is the total dielectric layer capacitance per unit area and ΔV_{th} is the memory window. The total stored charges per unit area were 3.63×10^{-7} C/cm^2 for S-OM and 5.82×10^{-7} C/cm^2 for D-OM, respectively. Hence, the numbers of trapped charge per Au NP were calculated to be 51.6–94.6 for S-OM and 28.8–36.7 for D-OM, respectively.[23] It reveals that the memory windows of organic memory devices were proportional to the spatial density of Au NPs in multi-stacked charge trapping layers. Therefore, memory capacity of organic memory devices could be remarkably increased by vertically stacking of a BCP layer with metal NPs and an insulating layer. Furthermore, as can be seen in Fig. 4, our memory devices have excellent durability, as tested by monitoring the on- and off-state I_{DS} and ΔV_{th} at each sweep cycles (up to 100 cycles).

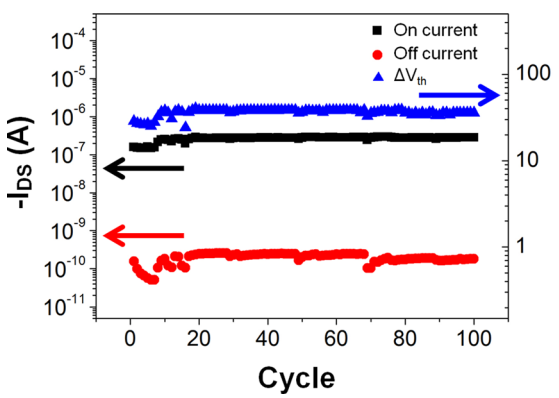

FIG. 4. Durability of D-OM devices employed in this study as a function of sweep cycles, V_G was dual swept from +20 V to −40 V at constant $V_{DS} = -60$ V.

In conclusion, we fabricated organic memory devices with multi-layered nanocomposite dielectrics formed by patterned Au NPs on a BCP layer. When bi-directional V_G sweeps were applied, the organic transistor devices exhibited counter-clockwise hysteresis, indicating that the memory characteristics were originated from hole trapping at the Au NPs. Organic memory devices with double nanocomposite dielectric layers showed a large memory window as well as excellent durability under repeated memory cycles. The bias hysteresis was increased in proportion to the total number of Au NPs in charge trapping dielectrics. Therefore, memory capacity could be significantly increased by vertical stacking of the alternating BCP layer with metal nano-floating-gates and photo-crosslinking dielectric layer. This can be a promising methodology for developing printed and flexible multi-level flash memory with large data storage capacity.

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[1]P. Heremans, G. H. Gelinck, R. Müller, K. J. Baeg, D. Y. Kim, and Y. Y. Noh, Chem. Mater. **23**, 341 (2011).
[2]X. Gao, X. J. She, C. H. Liu, Q. J. Sun, J. Liu, and S. D. Wang, Appl. Phys. Lett. **102**, 23303 (2013).
[3]Th. B. Singh, N. Marjanvić, G. J. Matt, N. S. Sariciftci, R. Schwödiauer, and S. Bauer, Appl. Phys. Lett. **85**, 5409 (2004).
[4]K. N. N. Unni, R. de Bettignies, D. S. Sylvie, and J. M. Nunzi, Appl. Phys. Lett. **85**, 1823 (2004).
[5]K.-J. Baeg, Y.-Y. Noh, J. Ghim, S.-J. Kang, H. Lee, and D.-Y. Kim, Adv. Mater. **18**, 3179 (2006).
[6]C. W. Tseng and Y. T. Tao, J. Am. Chem. Soc. **131**, 12441 (2009).
[7]Z. Liu, F. Xue, Y. Su, Y. M. Lvov, and K. Varahramyan, IEEE Trans. Nanotechnol. **5**, 379 (2006).
[8]W. Wang and D. Ma, Appl. Phys. Lett. **96**, 203304 (2010).
[9]K. S. Yook, S. O. Jeon, C. W. Joo, J. Y. Lee, S. H. Kim, and J. Jang, Org. Electron. **10**, 48 (2009).

[10]D. I. Son, J. H. Kim, D. H. Park, W. K. Choi, F. Li, J. H. Ham, and T. W. Kim, Nanotechnology **19**, 055204 (2008).
[11]J. Ouyang, C-W. Chu, C. R. Szmanda, L. Ma, and Y. Yang, Nat. Mater. **3**, 918 (2004).
[12]S. Kolliopoulou, P. Dimitrakis, P. Normand, H.-L. Zhang, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, and D. Tsoukalas, Microelectron. Eng. **73–74**, 725 (2004).
[13]C. O. Baker, B. Shedd, R. J. Tseng, A. A. Martinez-Morales, C. S. Ozkan, M. Ozkan, Y. Yang, and R. B. Kaner, ACS Nano **5**, 3469 (2011).
[14]D. U. Lee, M. S. Lee, J. H. Kim, E. K. Kim, H. M. Koo, W. J. Cho, and W. M. Kim, Appl. Phys. Lett. **90**, 093514 (2007).
[15]Y. Zhou, S. T. Han, Z. X. Xu, and V. A. L. Roy, Nanotechnology **23**, 344014 (2012).
[16]J. Y. Ouyang, C. W. Chu, R. J. H. Tseng, A. Prakash, and Y. Yang, Proc. IEEE **93**, 1287 (2005).
[17]W. L. Leong, N. Mathews, S. Mhaisalkar, Y. M. Lam, T. Chen, and P. S. Lee, J. Mater. Chem. **19**, 7354 (2009).
[18]M. Kang, K.-J. Baeg, D. Khim, Y.-Y. Noh, and D.-Y. Kim, Adv. Funct. Mater. **23**, 3503 (2013).
[19]G. Kästle, H.-G. Boyen, F. Weigl, G. Lengl, T. Herzog, P. Ziemann, S. Riethmüller, O. Mayer, C. Hartmann, J. P. Spatz, M. Möller, M. Ozawa, F. Banhart, M. G. Garnier, and P. Oelhafen, Adv. Funct. Mater. **13**, 853 (2003).
[20]W. L. Leong, P. S. Lee, A. Lohani, Y. M. Lam, T. Chen, S. Zhang, A. Dodabalapur, and S. G. Mhaisalkar, Adv. Mater. **20**, 2325 (2008).
[21]A. Horechyy, B. Nandan, N. E. Zafeiropoulos, P. Formanek, U. Oertel, N. C. Bigall, A. Eychmüller, and M. Stamm, Adv. Funct. Mater. **23**, 483 (2013).
[22]S. W. Ryu, J. W. Lee, J. W. Han, S. Kim, and Y. K. Choi, IEEE Trans. Electron Devices **56**, 377 (2009).
[23]Y. M. Kim, S. J. Kim, and J. S. Lee, IEEE Trans. Electron Device Lett. **31**, 503 (2010).
[24]C. Kim, A. Facchetti, and T. J. Marks, Science **318**, 76 (2007).
[25]Y. Wang, O. Acton, G. Ting, T. Weidner, P. J. Shamberge, H. Ma, F. S. Ohuchi, D. G. Castner, and A. K.-Y. Jen, Org. Electron. **11**, 1066 (2010).
[26]S. E. Fritz, T. W. Kelley, and C. D. Frisbie, J. Phys. Chem. B **109**, 10574 (2005).