Superhydrophobic modification of gate dielectrics for densely packed pentacene thin film transistors

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Superhydrophobic modification of gate dielectrics for densely packed pentacene thin film transistors

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Pentacene organic thin film transistors (OTFTs) with low-k and high-k hybrid gate dielectrics by CF_4 plasma treatment exhibited excellent device performance with field effect mobilities (maximum 1.41 $cm^2/V\,s$), a low threshold voltage of +1 V, and on/off current ratios of 10^5 at −5 V gate bias. After CF_4 plasma treatment, fluorine atoms diffuse into the interior low-k polymer and eliminate ionic impurities which reduce the leakage current density and overall pentacene initial growth on the superhydrophobic surface is significantly improved. It seems apparent that proper surface treatment is desirable for higher quality pentacene film and improving the performance of OTFTs. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2767779]

Organic thin film transistors (OTFTs) are an important class of electronic devices because they can potentially be developed into lightweight, flexible, and low cost electronic devices that can be fabricated with low temperature processes. A number of applications have been identified for OTFTs, including active matrix flexible displays, electronic paper, smart cards, radio frequency identification devices, and low cost disposable sensor arrays.[1,2] Especially, pentacene based TFTs represent particular interest as one of the most promising technologies. It is well known that carrier transport in polycrystalline pentacene films depends strongly on the surface properties of gate dielectrics which determine potential improvements in electronic characteristics of OTFTs.[3,4] It is therefore important to establish precise interfacial control between organic semiconductors/gate dielectrics in order to achieve higher performance in OTFTs.

CF_4 plasma treatments have been widely used to modify surface or define patterns in organic polymer films.[5–7] Unlike other plasmas, a fluorine containing plasma modifies not only the surface of low-k polymer but also their bulk properties. These changes manifest themselves, for example, superhydrophobicity of surface and reduction of leakage current density. In this study, we demonstrate that CF_4 plasma treatment of gate dielectrics can be significantly improved on the performance of OTFTs. Our pentacene TFTs with low-k and high-k hybrid gate dielectrics by CF_4 plasma treatment exhibited excellent device performance under low operating voltage conditions (less than −5 V) with field effect mobilities (maximum 1.41 $cm^2/V\,s$), a low threshold voltage of 1 V, and on/off current ratios of 10^5, respectively.

Recently, several experimental groups have reported that an attractive alternative approach for modifying gate dielectric surfaces is to deposit a second layer. This bilayer gate dielectric strategy is a general approach to enhancing charge carrier mobility, whether there is a correlation between organic semiconductors/polymer combination and OTFTs performance, and the nature of the gate dielectrics surface chemical factors underlying such interfacial effect on charge transport.[8,9] Figure 1(a) shows the schematic drawing of our pentacene TFTs (length, $L=100\ \mu m$, width, $W=1000\ \mu m$) structure. The preparation of PVP/CeO_2-SiO_2 films has

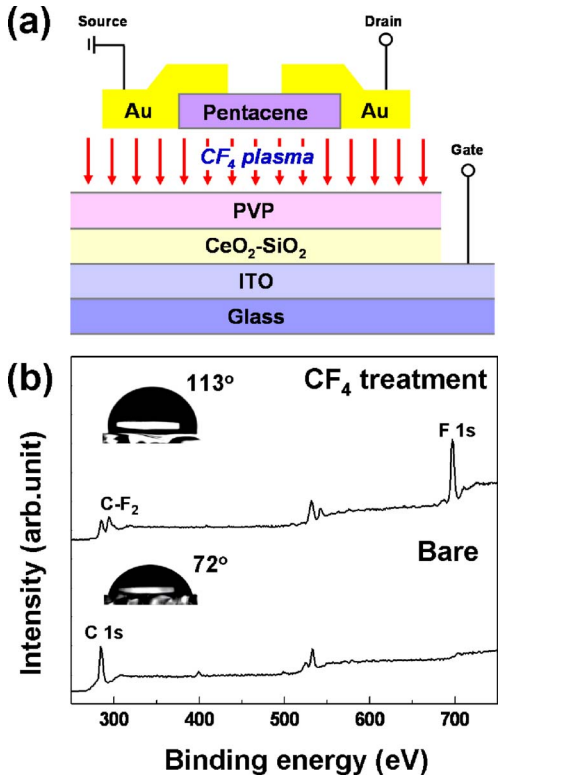

FIG. 1. (Color online) (a) Schematic structure of the fabricated top-contact pentacene TFTs with CF_4 plasma treatment. (b) Long scan x-ray photoelectron spectrum of PVP layer before and after CF_4 plasma treatment.

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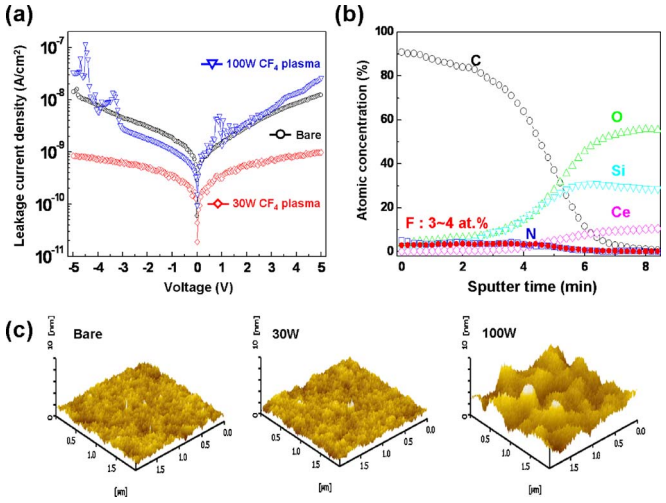

FIG. 2. (Color online) (a) Leakage current density of hybrid gate dielectrics treated at various CF_4 plasma powers. (b) AES depth profiles identifying fluorine incorporation in hybrid gate dielectrics after 30 W CF_4 plasma treatment. (c) AFM images of PVP layers treated at various CF_4 plasma powers.

been described in detail previously.[10,11] After PVP/CeO_2-SiO_2 gate dielectric deposition, CF_4 plasma was treated on top of PVP surface for 1 min at 30–100 W. The electrodes were made of Cu and have dimensions 5cm $\times$10cm. The pressure of the chamber and the flow rate of the CF_4 gas were 150 mTorr and 15 SCCM, respectively.

Figure 1(b) shows a long scan XPS curve of PVP layer before and after CF_4 plasma treatment. As shown in Fig. 1(b), the intensity of sp^2 (284.3 eV) carbon after CF_4 plasma treatment becomes broader in width and significantly reduced in intensity, at the same time a strong F 1*s* peak appears near 687 eV. In addition, the peak with 290.1 eV was ascribed to CF_2 bond. It is apparent that the low surface energy imparted by fluorine chemical species is necessary components to achieve a superhydrophobic surface.[12,13] A significant increase in the contact angle of DI water and diiodomethane as probe liquid on the CF_4 plasma treated PVP surface was observed. In the case of DI water, a contact angle was gradually increased from 72° to 113°, this highest contact angle was closer to the angle of 110° for Teflon. The measured surface energies of bare PVP layer and CF_4 plasma treated PVP layer were 26.92 and 17.48 mJ/m^2, respectively.

Figure 2(a) shows the leakage current density of hybrid gate dielectrics treated at various CF_4 plasma powers. The leakage current density of the bare gate dielectrics was about 10^{-8} A/cm^2 at −5 V. After 30 W CF_4 plasma treatment, leakage current density of the gate dielectrics exhibits one order of magnitude lowers than that bare gate dielectrics. Insulating materials such as PVP may contain mobile ions (e.g., H^+, Na^+, Cl^-, OH^-, etc.)[14] In fact, the ionic conduction of insulating polymer has been described, in terms of protons (H^+) in the PVP layer that act as carriers for ionic conduction. This suggests that the leakage current density was reduced by hydrogen ions combining with fluorine atoms to form HF.[15] Figure 2(b) shows the AES depth profiles of hybrid gate dielectrics after 30 W CF_4 plasma treatment. The fluorine content in the PVP layer after 30 W CF_4 plasma treatment was approximately 3%–4%, and fluorine atoms almost entirely distributed in the PVP layer. Thus, it appears that fluorine atoms diffuse into the interior PVP layer and eliminate ionic impurities which reduce the leakage current density. On the other hand, the gate capacitance of hybrid gate dielectrics was not obviously changed with CF_4 plasma treatment. As shown in Fig. 2(a), leakage current density of the gate dielectrics was improved with 30 W plasma power, but leakage current density was deteriorated in samples treated at 100 W. This phenomenon was related with an increase of leakage current density by an increase of film roughness. Figure 2(c) shows the surface morphology of PVP layers treated at various CF_4 plasma powers. As expected, the bare and 30 W plasma treated PVP surface exhibit a constant root mean square (rms) roughness of about 0.4 nm, but the PVP surface treated at 100 W shows rms roughness of about 2.1 nm.

As a necessary step before pentacene deposition, surface treatment of gate dielectrics can influence the pentacene morphology and the device performance greatly. However, the role of the gate dielectric surface treatment is not entirely clear and may be a surface energy and smoothness. Yang *et al.* have reported that the surface energy of polymer gate dielectrics significantly affected the morphology of pentacene films, in particular, the growth mode of pentacene (with similar surface roughness of gate dielectrics).[16,17] In spite of the small grain size and three dimensional (3D) growth on the gate dielectrics with low surface energy, the mobility of OTFTs with low surface energy gate dielectrics is larger compared to their high surface energy counterparts. They have suggested that the uniformity of the surface coverage is more important than the density of the grain boundaries in determining the charge mobility of OTFTs. This correlation between the surface coverage dependent mobility and the morphological evolution is crucial to the enhancing process of the charge mobility in 3D grown pentacene TFTs because they provide efficient percolation pathways for charge carriers. Figure 3 shows AFM images of 0.5 and 5 nm pentacene films deposited on bare PVP layer and CF_4 plasma treated PVP layer. It is well known that the current flow in OTFTs is mainly confined within the first 5 nm of semiconductor away from the gate dielectric/semiconductor interface. We found that the initial growth of the pentacene films at the interface is strongly affected by the surface wetting properties of the gate dielectrics. Larger pentacene grain sizes resulting from growth on bare PVP layer exhibit the large density of voids in the initial growth and we expect the carrier transport will be degraded significantly by the voids. On the contrary, pentacene grain size on CF_4 plasma treated PVP layer was markedly smaller than on bare PVP layer with fewer voids and improved contact between individual grains. The AFM images strongly suggest that the overall surface coverage of the initial growth was significantly improved on the superhydrophobic surface by the CF_4 plasma treatment.

Figures 4(a) and 4(b) show the drain current-drain voltage curves (I_D-V_D) obtained from pentacene TFTs fabricated on bare hybrid gate dielectrics and CF_4 plasma treated hybrid gate dielectrics, respectively. Both types of devices successfully demonstrated desirable TFT characteristics at an operating voltage lower than −5 V. Maximum saturation current of ~8 μA was achieved under a gate bias (V_G) of −5 V from the OTFTs with the bare hybrid gate dielectrics while about ~15 μA was achieved from the other OTFT with CF_4 plasma treated hybrid gate dielectrics. Although the capacitances of both hybrid gate dielectrics were similar, larger drain current was obtained due to high quality pentacene

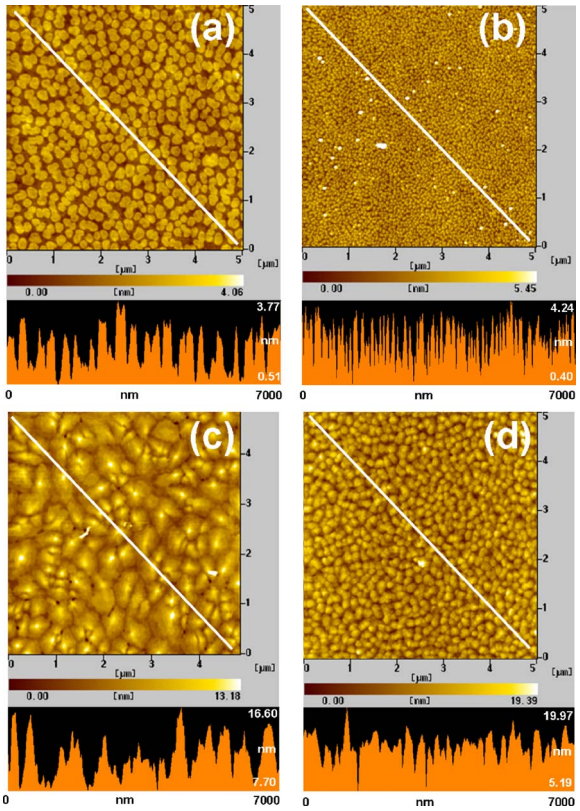

FIG. 3. (Color online) AFM images and height profiles of the 0.5 nm pentacene films deposited on (a) bare PVP layer and (b) 30 W CF_4 plasma treated PVP layer, and 5 nm pentacene films deposited on (c) bare PVP layer and (d) 30 W CF_4 plasma treated PVP layer.

films on CF_4 plasma treated hybrid gate dielectrics. From these results, it can be concluded that the voids and contact between individual grains at the interface affect the electrical characteristics of OTFTs. Field effect mobilities were determined from the $\sqrt{-I_D}$ vs V_G curves, as shown in Fig. 4(c). The field effect mobilities for the device with bare and CF_4 plasma treated hybrid gate dielectrics were 0.82, 1.41 $cm^2/V\,s$, respectively. These mobilities are also considerably increased with CF_4 plasma treated hybrid gate dielectrics due to improved carrier transport behavior on pentacene channel/dielectric interface. According to the plots of $\log_{10}(I_D)$-V_G, the on/off current ratios for each devices with bare and CF_4 plasma treated hybrid gate dielectrics were 10^4 and 10^5, respectively, reflecting the leakage current results of Fig. 2(a). The threshold voltage (V_T) of pentacene TFTs moved toward a more positive bias with CF_4 plasma treated hybrid gate dielectrics. The positive V_T is consistent with the presence of a permanent electric charges at the CF_4 plasma treated interface.[18,19]

In this study, we have fabricated pentacene TFTs with low-k and high-k hybrid gate dielectrics by CF_4 plasma treatment exhibited excellent device performance with field effect mobilities (maximum of 1.41 $cm^2/V\,s$), a low threshold voltage of +1 V, and on/off current ratios of 10^5 at −5 V gate bias. The result shows that the overall surface coverage of the initial pentacene growth was significantly improved on the superhydrophobic surface by the CF_4 plasma treatment and fluorine from the CF_4 plasma into the PVP layer to form HF bonding by CF_4 plasma treatment, resulting in the reduction of gate leakage current. More uniform surface coverage with fewer voids dominates over the density of grain boundaries in determining the electrical characteristics of OTFTs. Therefore, it seems apparent that proper surface treatment is desirable for higher quality pentacene film and improving the performance of OTFTs.

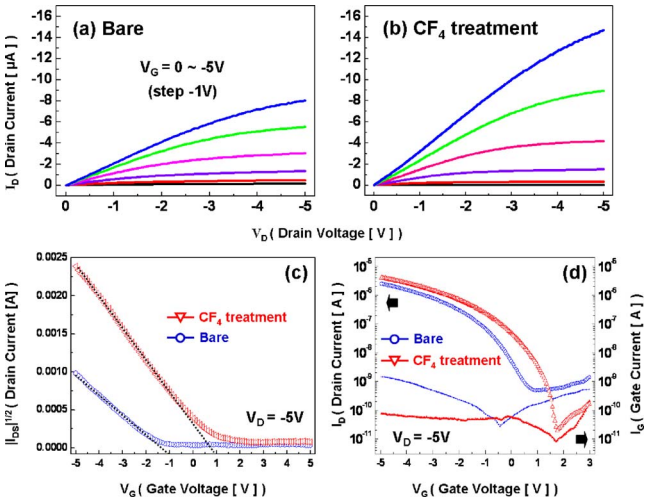

FIG. 4. (Color online) I_D-V_D curves at various V_G obtained from pentacene TFTs fabricated on (a) bare hybrid gate dielectrics and (b) CF_4 plasma treated hybrid gate dielectrics. (c) $\sqrt{I_D}$-V_G and (d) $\log_{10}(I_D)$-V_G curves for the estimation of saturation regime mobility that were obtained at V_D=−5 V from TFTs with pentacene TFTs fabricated on hybrid gate dielectrics before and after 30 W CF_4 plasma treatment.

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