Surface property controllable multilayered gate dielectric for low voltage organic thin film transistors

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Surface property controllable multilayered gate dielectric for low voltage organic thin film transistors

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We report the effects of dielectric surface properties on the device performance of organic thin film transistors (OTFTs) using polymer/high-*k* oxide multilayered gate dielectrics. We systematically controlled the surface energy of the gate dielectric from very hydrophobic to very hydrophilic. The modified dielectric surface strongly affected the initial growth mechanism of pentacene and subsequently the performance of the OTFTs. The performance of the OTFTs with a higher surface energy was superior to that of the OTFTs with a lower surface energy. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2973160]

Organic thin film transistors (OTFTs) have been studied extensively over the past few decades and are expected to lead the future of organic electronics.[1] However, the high operating voltage (over 50 V), which is attributed to the low dielectric constant of the common organic dielectric layer, remains a limitation of OTFTs. Recently, we introduced polymer/high-*k* oxide double gate dielectrics to increase the gate capacitance as well as to retain the advantages from the both organic and inorganic dielectrics.[2,3] The dielectric surface chemical modification can dictate the electrical performance of OTFTs by influencing the morphology and structure of the active layer. It is therefore important to establish precise interfacial control between organic semiconductors/polymer gate dielectrics in order to achieve higher performance in low operating voltage OTFTs with a multilayered gate dielectric. However, only a few systematic studies have been carried out to reveal the effects of dielectric surface properties on the device performance of OTFTs using polymer/high-*k* oxide multilayered gate dielectrics.

In this study, poly(dimethyl siloxane) (PDMS)/high-*k* yttrium oxide (YO_x) was chosen as a multilayered gate dielectric layer. Since the amount of methyl group on the surface of a PDMS dielectric can be controlled by ultraviolet/ozone (UVO) treatment, we were able to systematically control the surface energy of the gate dielectric from very hydrophobic to very hydrophilic (contact angle of water is 5°–103°). Moreover, this method enabled us to avoid the problems associated with the use of different functional groups, which may provide completely different environments for the organic semiconductor growth.

For the fabrication of the OTFT, heavily doped *p*-Si wafers were used as the substrate and gate electrode. As the inorganic high-*k* dielectric, YO_x films were deposited by electron beam evaporation at room temperature. Sylgard 184 PDMS prepolymer was mixed thoroughly with its cross-linking catalyst (10:1 w/w) and diluted in trichloroethylene. The diluted PDMS was spin-cast onto a substrate. The UVO

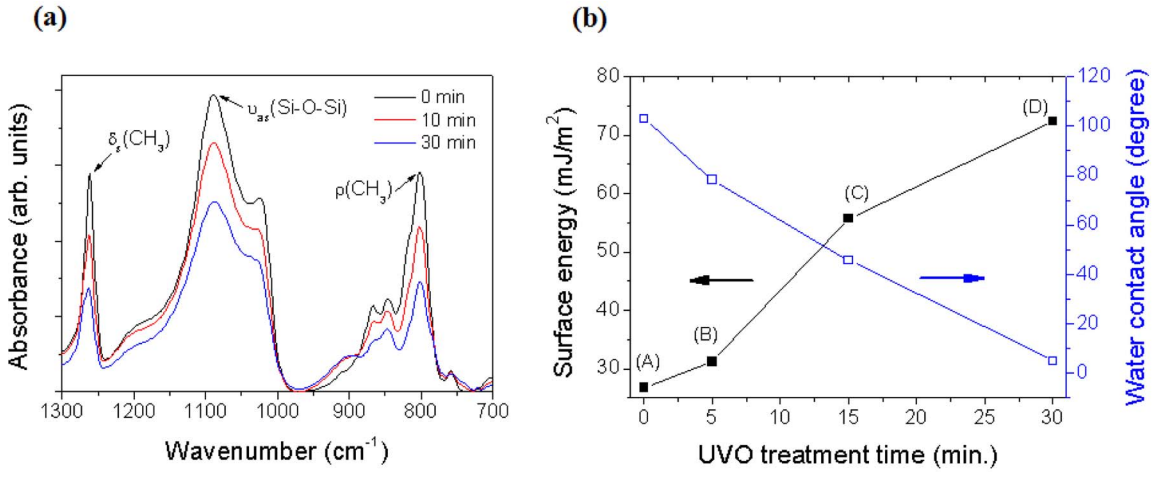

FIG. 1. (Color online) (a) FTIR transmission spectra of the PDMS layer at various UVO treatment times. (b) Surface energy and contact angle of water as a function of UVO treatment time for the PDMS layer. Gate dielectrics *A*, *B*, *C*, and *D* after UVO treatment times of 0, 5, 15, and 30 min, respectively.

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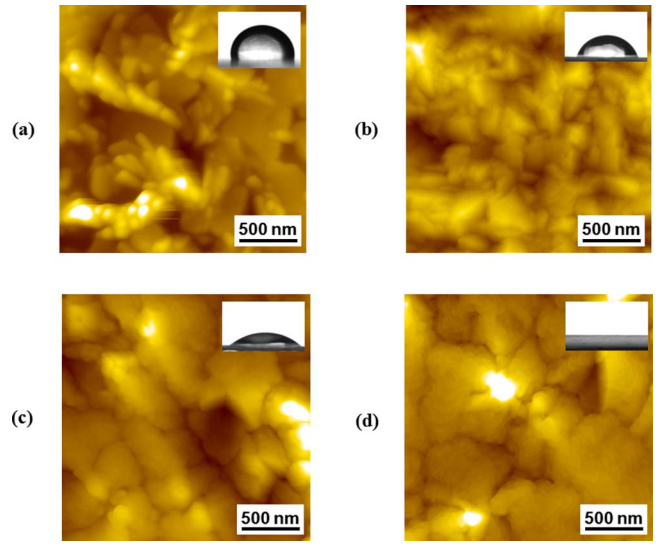

FIG. 2. (Color online) Tapping mode AFM topographic images of 50 nm thick pentacene films deposited on a PDMS/YO_x layer at various UVO treatment times: (a) UVO 0 min, (b) UVO 5 min, (c) UVO 15 min, and (d) UVO 30 min. Inset shows water droplet images on a PDMS/YO_x layer.

treatment of the PDMS surface was carried out in a commercial UVO surface treatment system (Minuta Tech, Ozone cure 16). Pentacene channels were deposited by heating the effusion cell. Finally, the gold was thermally evaporated to form the source/drain electrodes with a channel length of 100 μm and width of 2000 μm. The electrical characteristics of the OTFTs were measured using an Agilent 5270 B semiconductor parameter analyzer.

As shown in Fig. 1(a), Fourier transform infrared (FTIR) measurements were carried out on the PDMS layer in order to delineate the chemical state change of the PDMS layer by UVO treatment. Among the most intense were those associated with CH_3 rocking (785–815 cm^{-1}), symmetricCH_3 deformations (1245–1270 cm^{-1}), and asymmetric Si–O–Si stretches (1055–1090 cm^{-1}). UVO treatment caused a noticeable decrease in the magnitude of different CH_3 peaks, suggesting a gradual disappearance of methyl groups from oxidized molecules of PDMS.[4] To support the FTIR results, the surface energies of the PDMS layer at various UVO treatment times were measured using the sessile contact angle method. As shown in Fig. 1(b), an increase in the total surface energy in the PDMS layer was observed with an increased UVO treatment time. Gate dielectrics *A*, *B*, *C*, and *D* represent the PDMS layer after UVO treatments of 0, 5, 15, and 30 min, respectively. The FTIR and surface energy measurement results confirmed that the decrease in the number of methyl groups directly is related to the increase in the surface energy of the PDMS layer.

We expected that the difference in surface wetting properties caused by the methyl group density would strongly influence the pentacene growth morphology. Generally, in order to form large pentacene islands in the initial stages of growth, the gate dielectric is required to have a relatively high surface energy that can induce the increased wetting and two-dimensional growth of the pentacene film. Moreover, many reports have experimentally demonstrated that pentacene films grown on a hydrophilic surface form large grains.[5–7] Shin *et al.*[8] presented that the increased surface energy of a dielectric that results from the oxygen plasma ensures a good wetting of the pentacene on the dielectric surface and enlarges the grain size. As shown in Fig. 2, the pentacene films on dielectrics *C* and *D*, having higher surface energies, exhibited well-formed dendritic structures and grain sizes around 1–2 μm. However, on gate dielectric *B*, having a lower surface energy, the pentacene film did not show any dendritic structure and its grain size was reduced to less than 0.2 μm. Also, the pentacene film on dielectric *A* showed very rough surface morphology with inclined grains and many voids; this presumably occurred because the interaction between the pentacene and the CH_3-functional group was too severe.[9]

To correlate the pentacene morphology described above with the electrical properties of the OTFTs, transistors were fabricated. As shown in Fig. 3, all the TFT performance characteristics, particularly carrier mobility, were considerably improved as the UVO treatment time increased. The carrier mobilities of the TFTs with gate dielectrics *A*, *B*, *C*, and *D* were 0.002, 0.259, 0.897, and 2.124 $cm^2/V\,s$, respectively. As discussed above, the enhancement of carrier mobility may be attributed to the growth mode change of pentacene. A decrease in the grain size of the organic semiconductor reduces the carrier mobility of the OTFTs. It is clearly seen from Fig. 2 that the pentacene grain size increased as the UVO treatment time increased. Moreover, it is known that in the OTFTs, the carriers induced by the gate bias are located within a few monolayers just above the dielectric layers. Thus, to understand the origin of the mobility enhancement more precisely, the morphology of the pentacene film was investigated in detail during the initial growth step. Figure 4

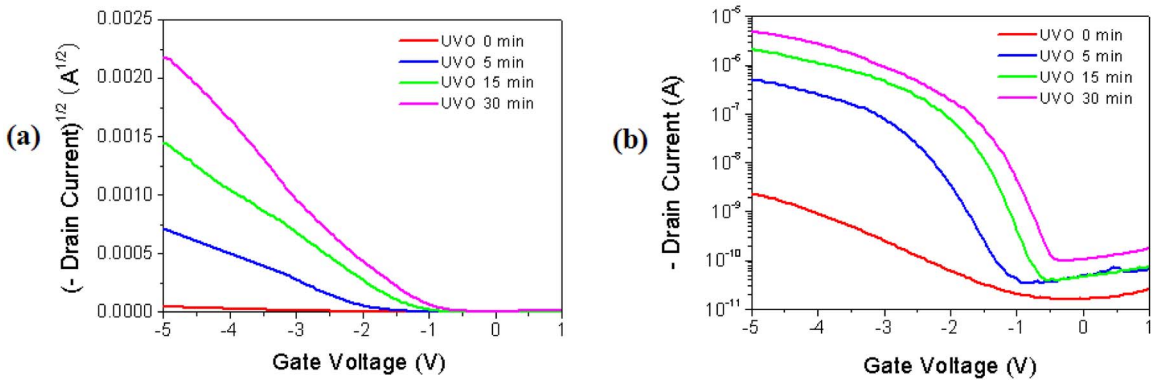

FIG. 3. (Color online) Transfer characteristics of pentacene TFTs fabricated on a PDMS/YO_x layer at various UVO treatment times: (a) $\sqrt{I_D}$-V_G and (b) $\log(I_D)$-V_G curves.

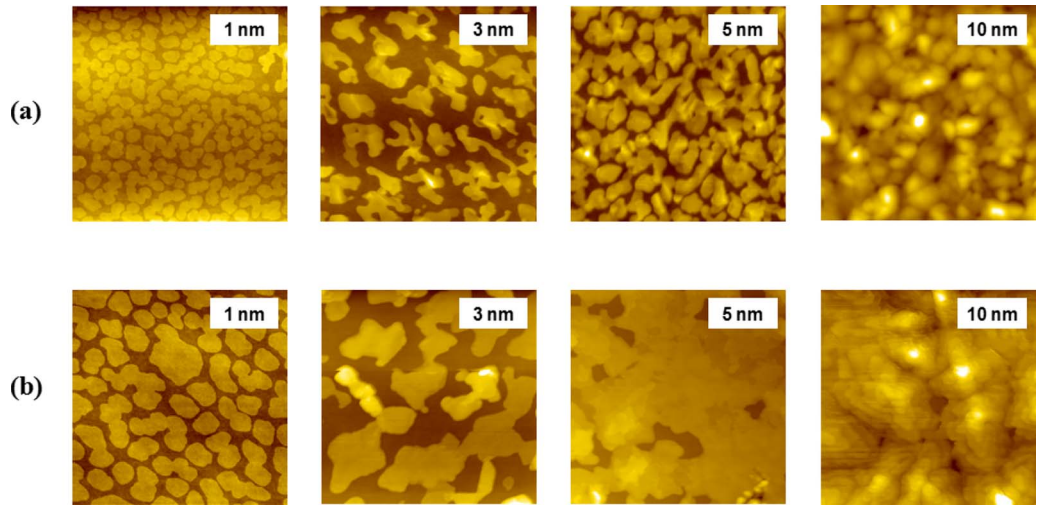

FIG. 4. (Color online) 2×2 μm^2 AFM images of pentacene films deposited on a PDMS/YO_x layer with nominal thicknesses of 1, 3, 5, and 10 nm, respectively. UVO treatments for (a) 5 min and (b) 15 min.

shows AFM images of the pentacene films grown on dielectrics *B* and *C* with nominal thickness increasing from 1 to 10 nm. The morphology of pentacene on gate dielectric *B* was strikingly different from that on gate dielectric *C*. On gate dielectric *B*, the process of island coalescence was more limited, whereas the adjacent islands coalesced to form larger islands in the case of gate dielectric *C*. The vacant space between islands did not decrease appreciably for the pentacene films on gate dielectric *B*, and large vacant spaces between grains were observed even at a film thickness of 5 nm. These results strongly suggest that different pentacene growth mechanisms are involved according to the surface state of the gate dielectric layer.

To provide a quantitative basis for the growth mode change of pentacene film on gate dielectrics *B* and *C*, we have calculated the work of adhesion between pentacene and the gate dielectric. Since the work of adhesion (W_a) between materials can be defined by the relationship involving surface energies and interfacial energy as follows, the Volmen–Weber mode is favored when $W_a<2\gamma_f$ and the Frank–van der Merwe mode is favored when $W_a>2\gamma_f$.[10]

$$W_a=\gamma_f+\gamma_s-\gamma_i=\frac{4\gamma_f^d\gamma_s^d}{\gamma_f^d+\gamma_s^d}-\frac{4\gamma_f^p\gamma_s^p}{\gamma_f^p+\gamma_s^p}, \quad (1)$$

where *d* and *p* represent the dispersion and polar components of the surface tension, respectively. The calculated works of adhesion from Eq. (1) are $W_a=66.0$ mJ/m^2 for pentacene and gate dielectric *B* and $W_a=83.2$ mJ/m^2 for pentacene and gate dielectric *C*. The surface energy of pentacene was also measured by the contact angle method and the value was 35.1 mJ/m^2. Thus, the Volmen–Weber mode was observed on gate dielectric *B*, while the Frank–van der Merwe mode was observed on gate dielectric *C*. Considering that charge transport occurs dominantly at a few pentacene monolayers, Frank–van der Merwe growth is desired for transistor applications because it leads to large, well-connected domains that facilitate a charge transport parallel to the substrate. Indeed, at a nominal thickness of 5 nm, the ratio of the grain area on dielectric *B* was increased from 68.7% to 88.7% on dielectric *C*. This indicated that the voids between the islands that disturb the carrier transport were reduced when the pentacene film was deposited on gate dielectric *C*.

In summary, we investigated the semiconductor/dielectric interface chemical effects on low voltage OTFT performance. The present results for OTFTs fabricated on multilayered gate dielectrics having a wide range of surface chemical states provide new insights into the critical relationships between OTFT performance parameters and semiconductor growth mechanisms.

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